

Model Name:GA-990XA-UD3

Component value change history

Version: 3.03

4 Layer, 4mil 50ohm +/- 15% L

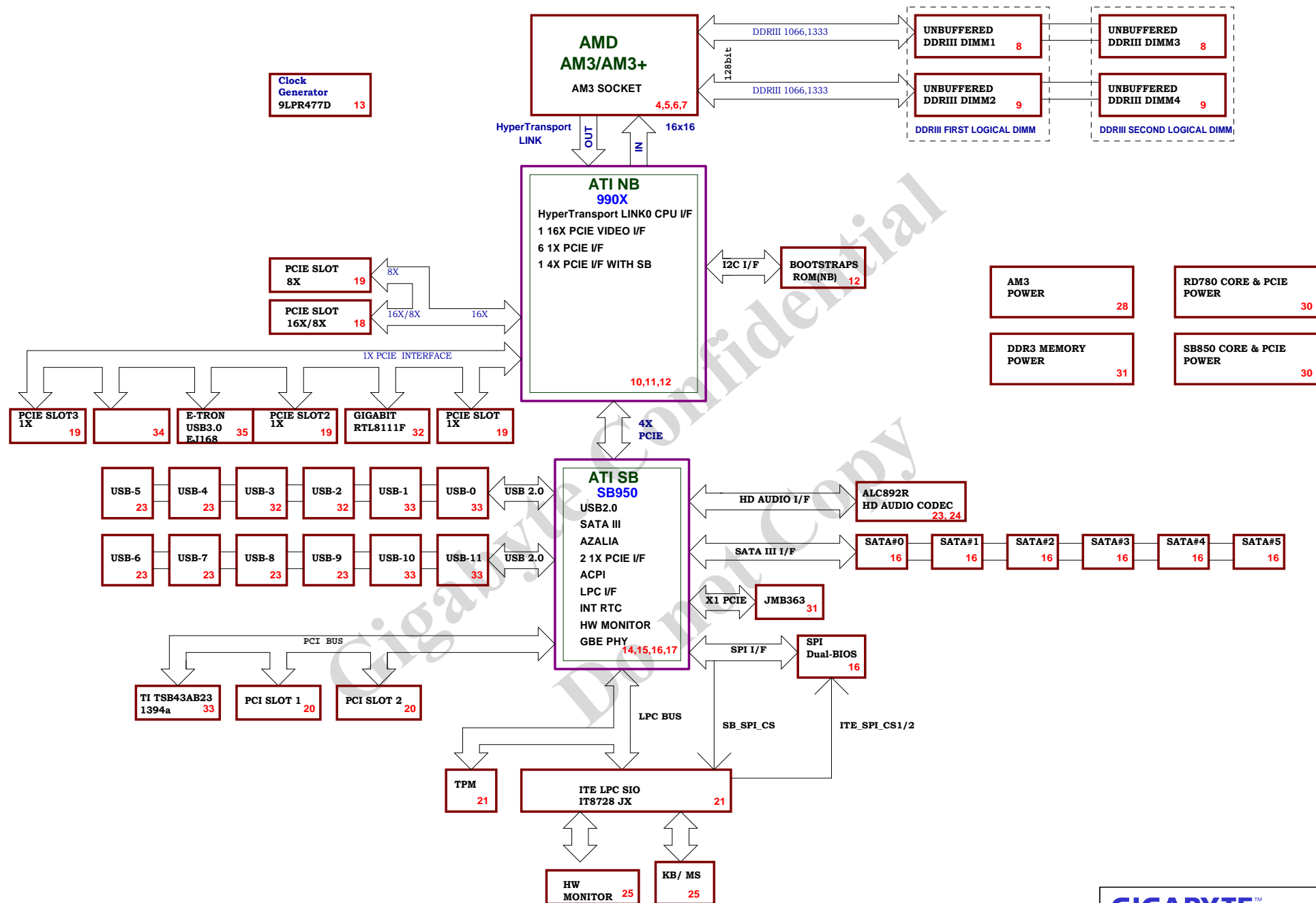
P-Code: U98094-0

[illegible]

Circuit or PCB layout change for next version

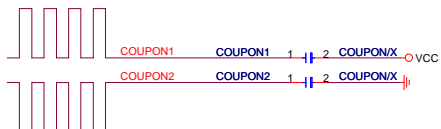
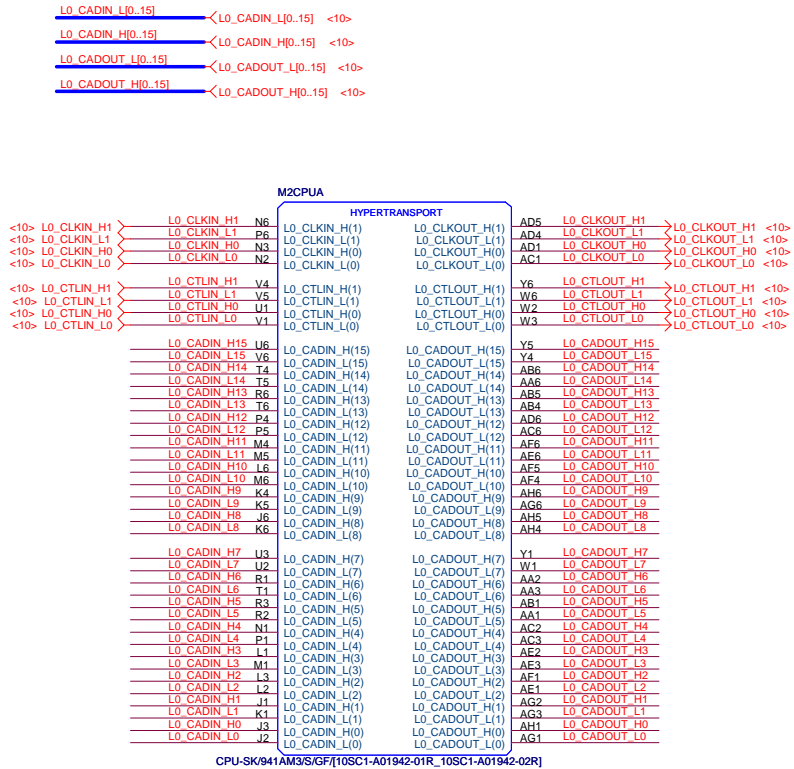
[illegible]**GIGABYTE™**

| | | | |
|------------------------------|------------------------------|-------------|---------|
| Title | | | |
| BOM & PCB HISTORY | | | |
| Size | Document Number | Rev | |
| Custom | GA-990XA-UD3 | 3.03 | |
| Date: | Wednesday, December 19, 2012 | Sheet | 2 of 35 |

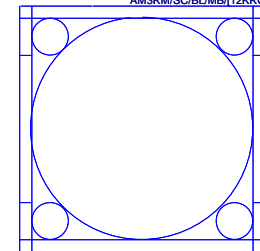


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

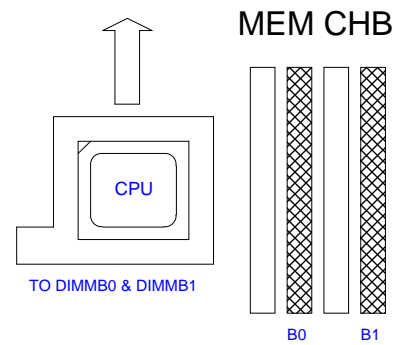
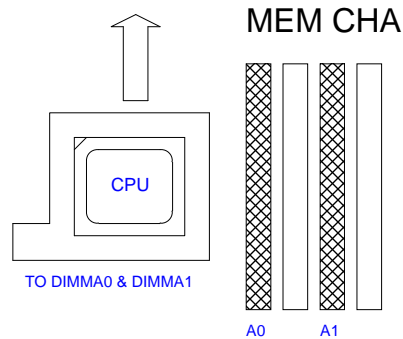
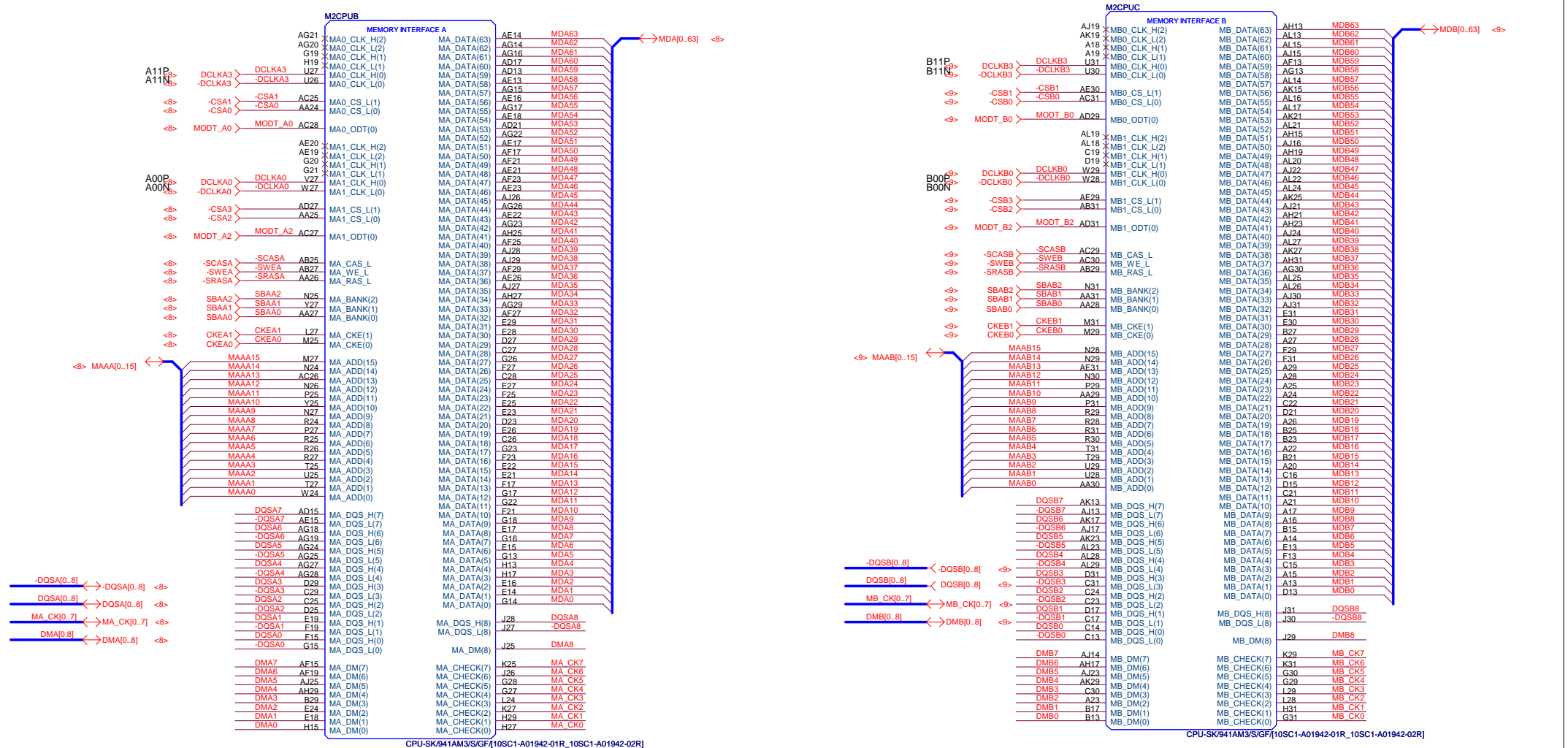
VLDT_A = VCC12_HT
 VLDT_B = HT12B

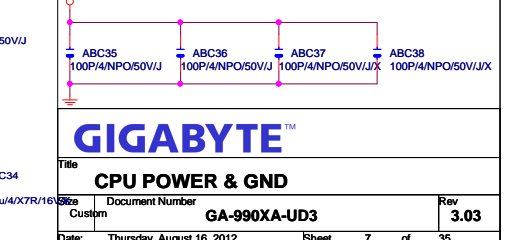
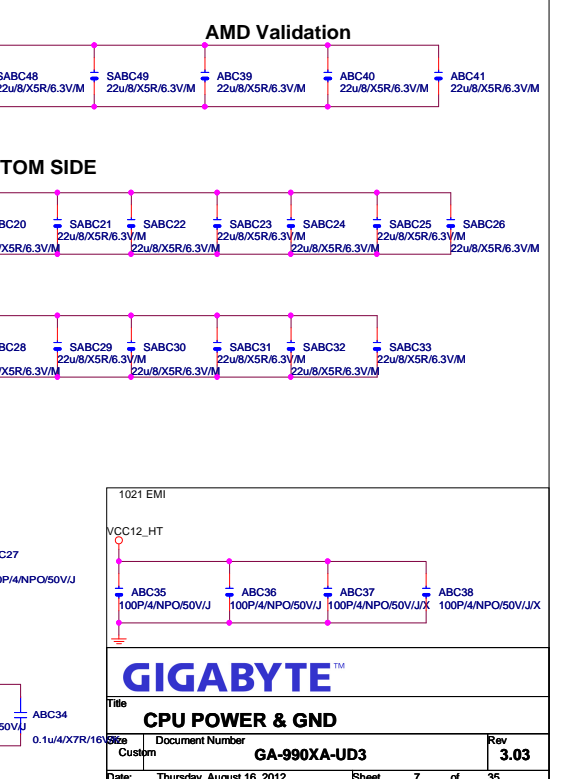
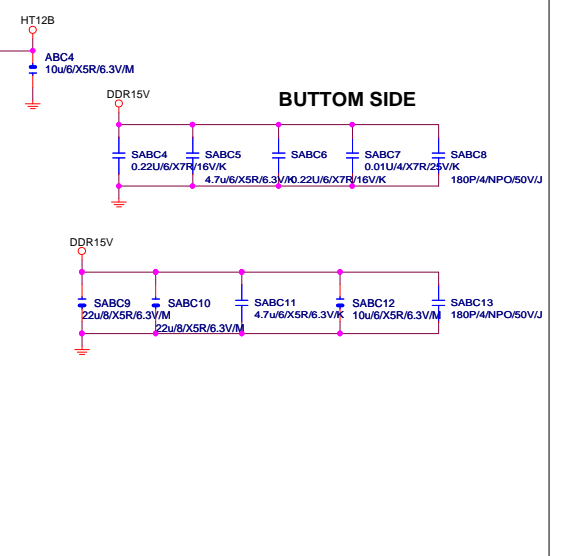


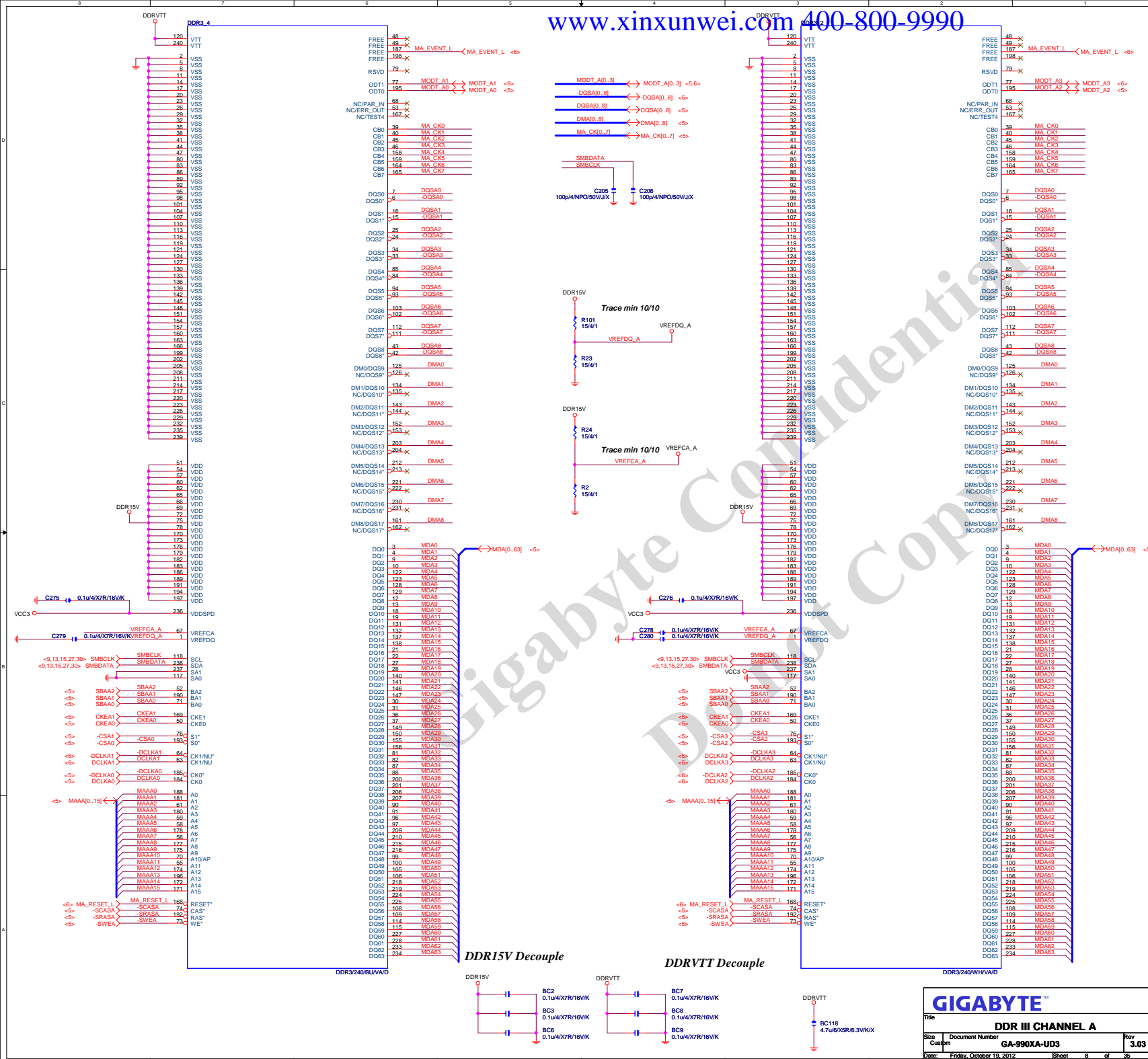
M2CPU
 AM3RM/SC/BL/MB/12KRC-04K812-31R]

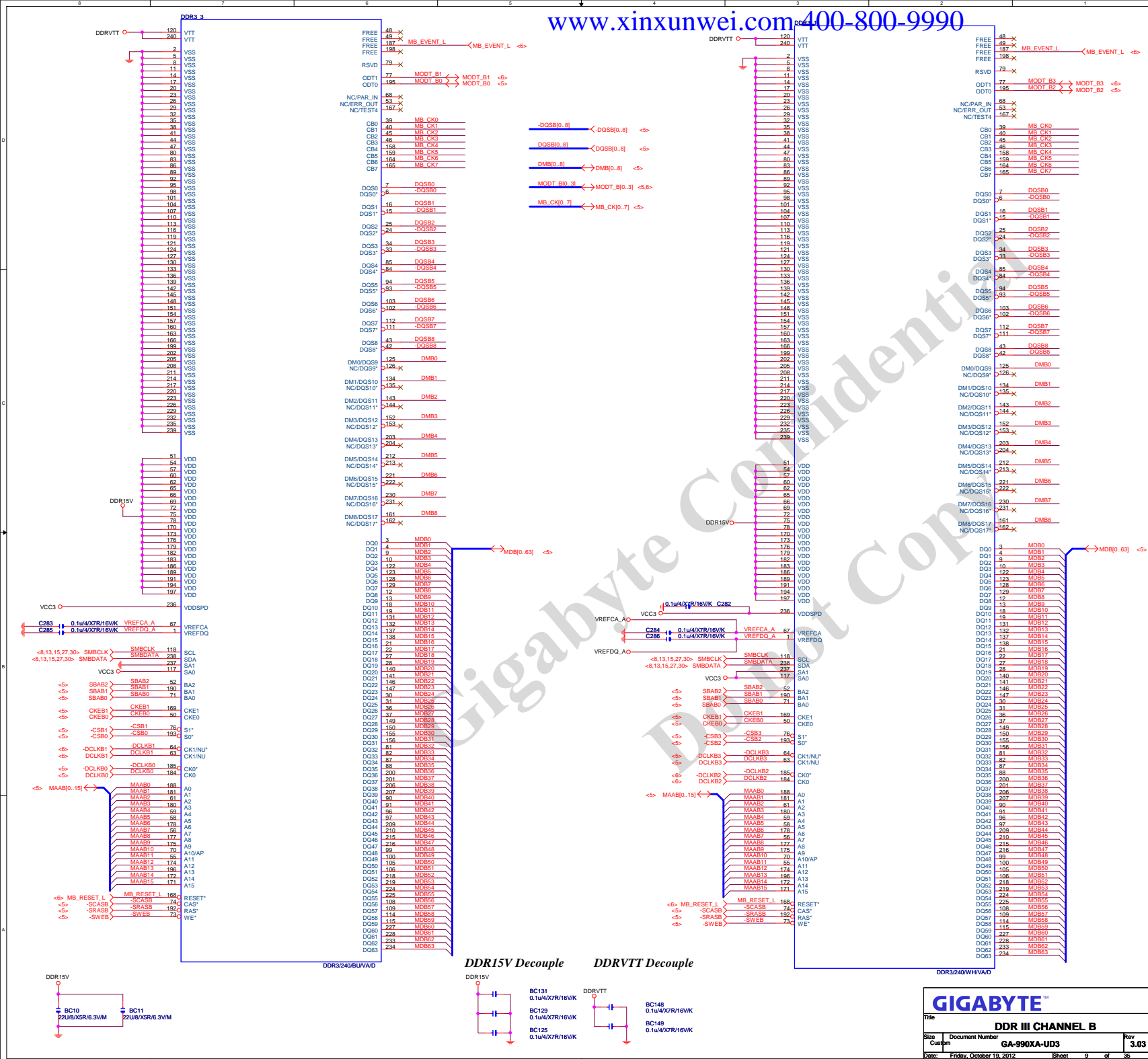


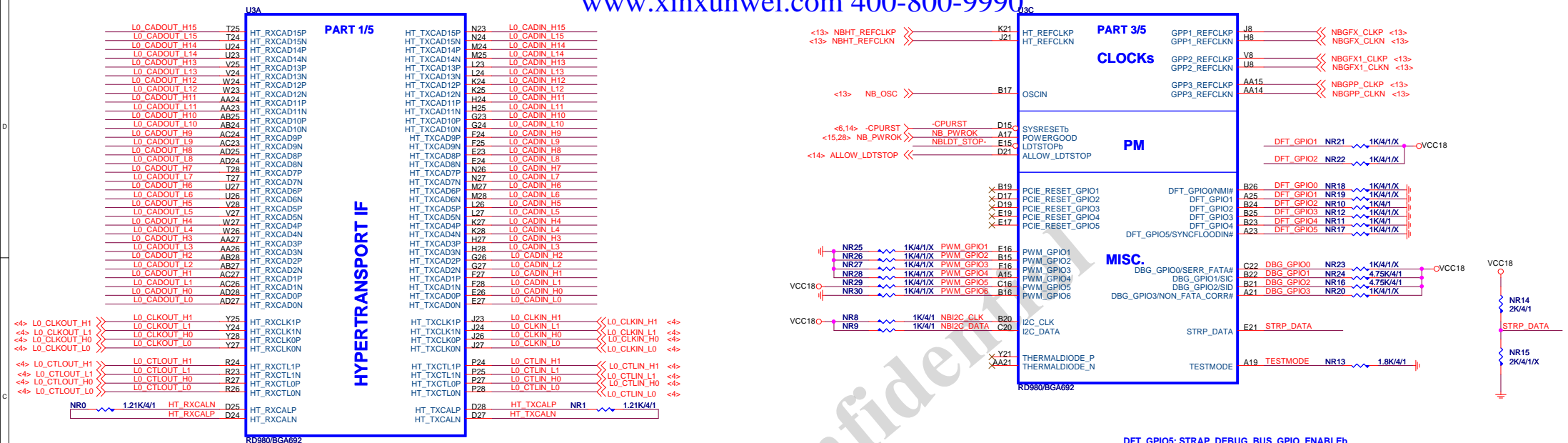
| GIGABYTE™ | | | |
|---------------------|--------------------------|-------|---------|
| Title | | | |
| CPU HYPER TRANSPORT | | | |
| Size | Document Number | Rev | |
| Custom | GA-990XA-UD3 | 3.03 | |
| Date: | Friday, October 19, 2012 | Sheet | 4 of 35 |











DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using
nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

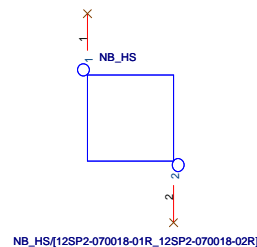
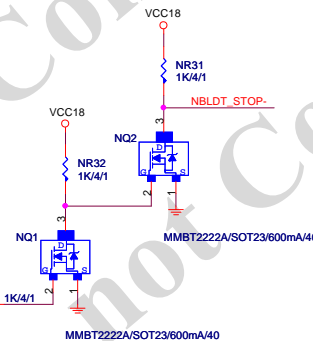
```
These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000: 4:2:4 B
001: 4:1:1:4 C
010: 1:1:1:1:1:4 L (Hardware Default)
011: 2:1:1:1:4 E
100: 2:2:1:1:4 K
101: 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101: 01100
111: 01011
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIe bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable





U3B

PART 2/5

| | | |
|-------------|-----|------------|
| EXP A_RXP15 | N6 | GPP1_RX15P |
| EXP A_RXN15 | M5 | GPP1_RX15N |
| EXP A_RXP14 | M5 | GPP1_RX14P |
| EXP A_RXN14 | M4 | GPP1_RX14N |
| EXP A_RXP13 | L6 | GPP1_RX13P |
| EXP A_RXN13 | L5 | GPP1_RX13N |
| EXP A_RXP12 | K4 | GPP1_RX12P |
| EXP A_RXN12 | K4 | GPP1_RX12N |
| EXP A_RXP11 | J6 | GPP1_RX11P |
| EXP A_RXN11 | J5 | GPP1_RX11N |
| EXP A_RXP10 | H4 | GPP1_RX10P |
| EXP A_RXN10 | H4 | GPP1_RX10N |
| EXP A_RXP9 | G6 | GPP1_RX9P |
| EXP A_RXN9 | G5 | GPP1_RX9N |
| EXP A_RXP8 | F5 | GPP1_RX8P |
| EXP A_RXN8 | F4 | GPP1_RX8N |
| EXP A_RXP7 | D2 | GPP1_RX7P |
| EXP A_RXN7 | D1 | GPP1_RX7N |
| EXP A_RXP6 | B5 | GPP1_RX6P |
| EXP A_RXN6 | B6 | GPP1_RX6N |
| EXP A_RXP5 | C6 | GPP1_RX5P |
| EXP A_RXN5 | E6 | GPP1_RX5N |
| EXP A_RXP4 | E7 | GPP1_RX4P |
| EXP A_RXN4 | F7 | GPP1_RX4N |
| EXP A_RXP3 | D8 | GPP1_RX3P |
| EXP A_RXN3 | E8 | GPP1_RX3N |
| EXP A_RXP2 | E9 | GPP1_RX2P |
| EXP A_RXN2 | F9 | GPP1_RX2N |
| EXP A_RXP1 | D10 | GPP1_RX1P |
| EXP A_RXN1 | E10 | GPP1_RX1N |
| EXP A_RXP0 | E11 | GPP1_RX0P |
| EXP A_RXN0 | F11 | GPP1_RX0N |

PCIE GPP1

| | |
|-----|------------|
| AC9 | GPP2_RX15P |
| AD9 | GPP2_RX15N |
| AE8 | GPP2_RX14P |
| AE7 | GPP2_RX14N |
| AD7 | GPP2_RX13P |
| AD6 | GPP2_RX13N |
| AE6 | GPP2_RX12P |
| AE5 | GPP2_RX12N |
| AG5 | GPP2_RX11P |
| AF2 | GPP2_RX11N |
| AD2 | GPP2_RX10P |
| AD1 | GPP2_RX10N |
| AB5 | GPP2_RX9P |
| AB4 | GPP2_RX9N |
| AA6 | GPP2_RX8P |
| AA5 | GPP2_RX8N |
| Y5 | GPP2_RX7P |
| Y4 | GPP2_RX7N |
| W6 | GPP2_RX6P |
| W5 | GPP2_RX6N |
| V5 | GPP2_RX5P |
| V4 | GPP2_RX5N |
| U6 | GPP2_RX4P |
| U5 | GPP2_RX4N |
| T5 | GPP2_RX3P |
| T4 | GPP2_RX3N |
| R6 | GPP2_RX2P |
| R5 | GPP2_RX2N |
| P5 | GPP2_RX1P |
| P4 | GPP2_RX1N |

PCIE GPP2

| | |
|------|-----------|
| AD11 | GPP3_RX9P |
| AC11 | GPP3_RX9N |
| AE12 | GPP3_RX8P |
| AD12 | GPP3_RX8N |
| AD13 | GPP3_RX7P |
| AC13 | GPP3_RX7N |
| AE14 | GPP3_RX6P |
| AD14 | GPP3_RX6N |
| AD15 | GPP3_RX5P |
| AC15 | GPP3_RX5N |
| AE16 | GPP3_RX4P |
| AD16 | GPP3_RX4N |
| AC17 | GPP3_RX3P |
| AE18 | GPP3_RX3N |
| AD18 | GPP3_RX2P |
| AC19 | GPP3_RX2N |
| AE19 | GPP3_RX1P |
| AD20 | GPP3_RX1N |
| AG20 | GPP3_RX0P |
| | GPP3_RX0N |

PCIE GPP3

| | |
|------|---------|
| AC21 | SB_RX3P |
| AD21 | SB_RX3N |
| AE22 | SB_RX2P |
| AD22 | SB_RX2N |
| AE25 | SB_RX1P |
| AD25 | SB_RX1N |
| AE26 | SB_RX0P |
| AD26 | SB_RX0N |

PCIE ALINK

RD980/BGA692

| | |
|-----|-------------|
| N3 | EXP A_TXP15 |
| M2 | EXP A_TXN15 |
| M1 | EXP A_TXP14 |
| L3 | EXP A_TXP13 |
| L2 | EXP A_TXN13 |
| K2 | EXP A_TXP12 |
| K1 | EXP A_TXN12 |
| J3 | EXP A_TXP11 |
| J2 | EXP A_TXN11 |
| H2 | EXP A_TXP10 |
| H1 | EXP A_TXN10 |
| G3 | EXP A_TXP9 |
| G2 | EXP A_TXN9 |
| F2 | EXP A_TXP8 |
| F1 | EXP A_TXN8 |
| E3 | EXP A_TXP7 |
| E2 | EXP A_TXN7 |
| A4 | EXP A_TXP6 |
| A6 | EXP A_TXN6 |
| B6 | EXP A_TXP5 |
| B7 | EXP A_TXN5 |
| C7 | EXP A_TXP4 |
| A8 | EXP A_TXN4 |
| B8 | EXP A_TXP3 |
| B9 | EXP A_TXN3 |
| C9 | EXP A_TXP2 |
| A10 | EXP A_TXN2 |
| B10 | EXP A_TXP1 |
| B11 | EXP A_TXN1 |
| C11 | EXP A_TXP0 |
| | EXP A_TXN0 |

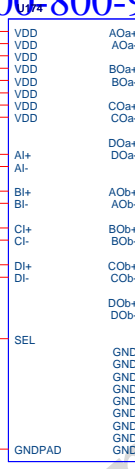
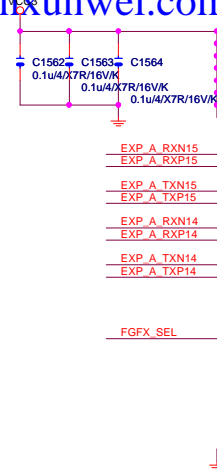
| | |
|-----|------------|
| AF9 | GPP2_TX15P |
| AG9 | GPP2_TX15N |
| AG8 | GPP2_TX14P |
| AH8 | GPP2_TX14N |
| AF7 | GPP2_TX13P |
| AG7 | GPP2_TX13N |
| AH6 | GPP2_TX12P |
| AG6 | GPP2_TX12N |
| AG4 | GPP2_TX11P |
| AH4 | GPP2_TX11N |
| AE3 | GPP2_TX10P |
| AE2 | GPP2_TX10N |
| AC3 | GPP2_TX9P |
| AC2 | GPP2_TX9N |
| AB2 | GPP2_TX8P |
| AB1 | GPP2_TX8N |
| AA3 | GPP2_TX7P |
| AA2 | GPP2_TX7N |
| Y2 | GPP2_TX6P |
| Y1 | GPP2_TX6N |
| W2 | GPP2_TX5P |
| W1 | GPP2_TX5N |
| V2 | GPP2_TX4P |
| V1 | GPP2_TX4N |
| U2 | GPP2_TX3P |
| U1 | GPP2_TX3N |
| T2 | GPP2_TX2P |
| T1 | GPP2_TX2N |
| R3 | GPP2_TX1P |
| R2 | GPP2_TX1N |
| P2 | GPP2_TX0P |
| P1 | GPP2_TX0N |

PCI E slot TX need CAP close to slot side

| | | | | |
|------------|------|-----------------|------------|------|
| GPP TX5P_C | NC4 | 0.1u/4X7R/16V/K | 168_OP | <31> |
| GPP TX5N_C | NC3 | 0.1u/4X7R/16V/K | 168_ON | <31> |
| GPP TX4P_C | NC6 | 0.1u/4X7R/16V/K | ML_OP | <34> |
| GPP TX4N_C | NC5 | 0.1u/4X7R/16V/K | ML_ON | <34> |
| GPP TX2P_C | | | GPP TX2P_C | <19> |
| GPP TX2N_C | | | GPP TX2N_C | <19> |
| GPP TX1P_C | | | GPP TX1P_C | <19> |
| GPP TX1N_C | | | GPP TX1N_C | <19> |
| GPP TX0P_C | NC2 | 0.1u/4X7R/16V/K | USB3_OP | <32> |
| GPP TX0N_C | NC1 | 0.1u/4X7R/16V/K | USB3_ON | <32> |
| A TX3P_C | NC11 | 0.1u/4X7R/16V/K | A TX3P | <14> |
| A TX3N_C | NC12 | 0.1u/4X7R/16V/K | A TX3N | <14> |
| A TX2P_C | NC14 | 0.1u/4X7R/16V/K | A TX2P | <14> |
| A TX2N_C | NC13 | 0.1u/4X7R/16V/K | A TX2N | <14> |
| A TX1P_C | NC15 | 0.1u/4X7R/16V/K | A TX1P | <14> |
| A TX1N_C | NC16 | 0.1u/4X7R/16V/K | A TX1N | <14> |
| A TX0P_C | NC18 | 0.1u/4X7R/16V/K | A TX0P | <14> |
| A TX0N_C | NC17 | 0.1u/4X7R/16V/K | A TX0N | <14> |

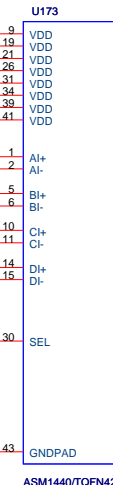
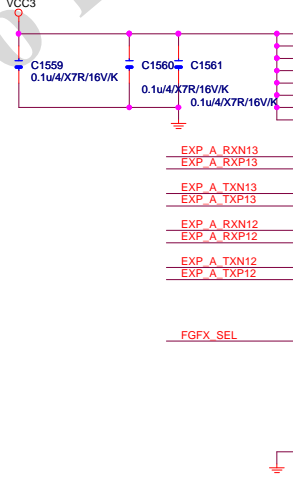
PLACE THESE CAP CLOSE TO NB.

| | | |
|-----|-----------|------|
| NR2 | 1.27K/4/1 | AE20 |
| NR3 | 1.82K/4/1 | AD20 |
| NR4 | 1.27K/4/1 | AE10 |
| NR5 | 1.82K/4/1 | AD10 |
| NR6 | 1.27K/4/1 | F14 |
| NR7 | 1.82K/4/1 | E14 |

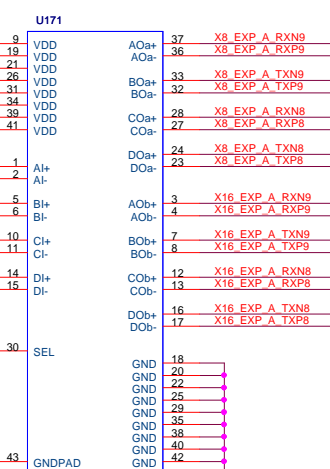
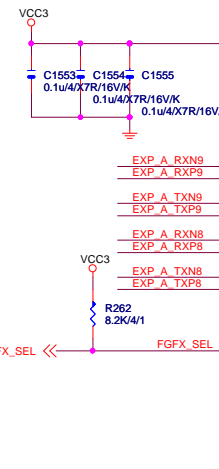
PCE_BCALRP
PCE_BCALRN
PCE_RCALRP
PCE_RCALRN
PCE_TCALRP
PCE_TCALRN

ASM1440/TQFN42

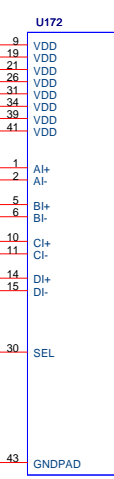
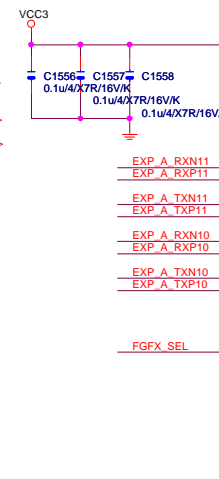
| | |
|----------------------|------------------------------|
| X16_EXP_A_TXP[8..15] | >>>X16_EXP_A_TXP[8..15] <18> |
| X16_EXP_A_TXN[8..15] | >>>X16_EXP_A_TXN[8..15] <18> |
| X16_EXP_A_RXP[8..15] | >>>X16_EXP_A_RXP[8..15] <18> |
| X16_EXP_A_RXN[8..15] | >>>X16_EXP_A_RXN[8..15] <18> |
| X8_EXP_A_TXP[8..15] | >>>X8_EXP_A_TXP[8..15] <19> |
| X8_EXP_A_TXN[8..15] | >>>X8_EXP_A_TXN[8..15] <19> |
| X8_EXP_A_RXP[8..15] | >>>X8_EXP_A_RXP[8..15] <19> |
| X8_EXP_A_RXN[8..15] | >>>X8_EXP_A_RXN[8..15] <19> |
| EXP_A_TXP[0..7] | >>>EXP_A_TXP[0..7] <18> |
| EXP_A_TXN[0..7] | >>>EXP_A_TXN[0..7] <18> |
| EXP_A_RXP[0..7] | >>>EXP_A_RXP[0..7] <18> |
| EXP_A_RXN[0..7] | >>>EXP_A_RXN[0..7] <18> |



ASM1440/TQFN42



ASM1440/TQFN42



ASM1440/TQFN42

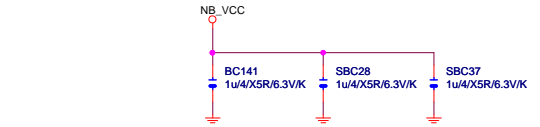
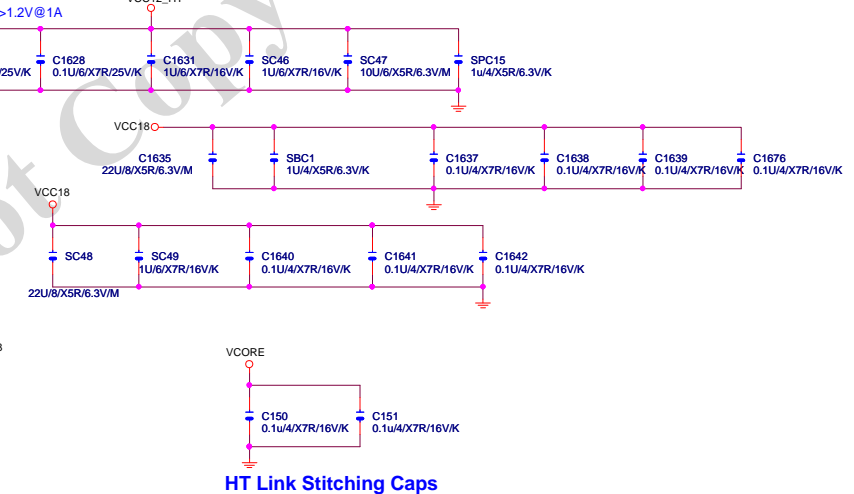
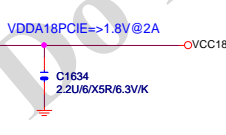
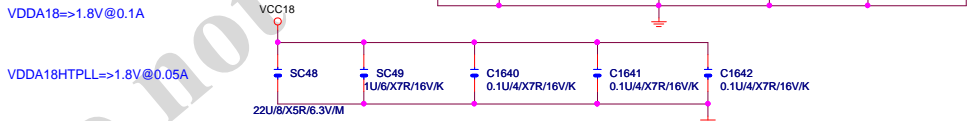
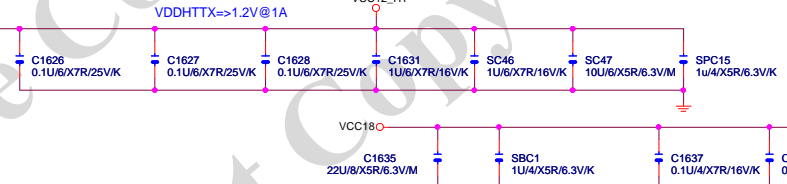
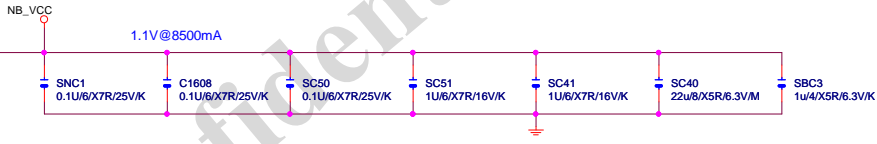
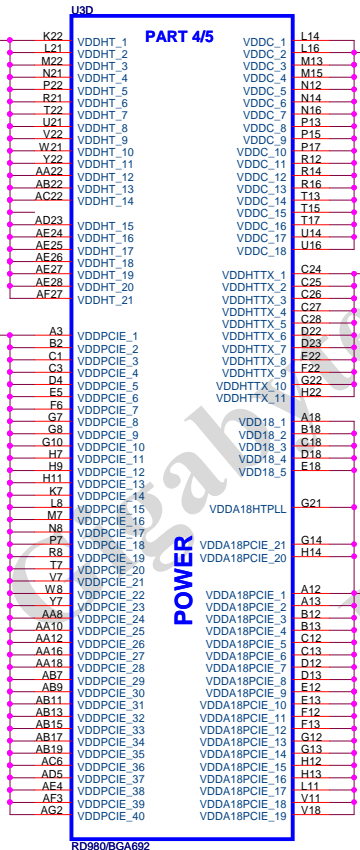
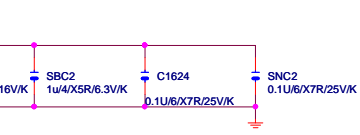
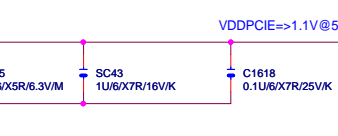
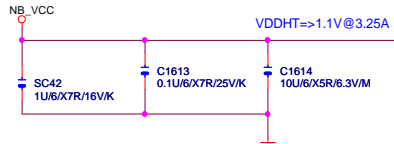
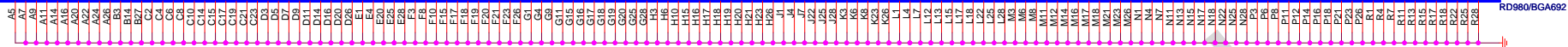
| Function | SEL |
|-----------|-----------|
| xI--> xOa | L (X8) |
| xI--> xOb | H (X16) |

GIGABYTE™

| | | | |
|--------|--------------------------|-------|----------|
| Title | RD990 PCIE I/F_Switch | Rev | 3.03 |
| Size | Document Number | | |
| Custom | GA-990XA-UD3 | | |
| Date | Friday, October 19, 2012 | Sheet | 11 of 35 |

PART 5/5

GROUND



NB CLOCK INPUT TABLE

| NB CLOCKS | RS740 | RX780 | RS780 | |
|--------------|---------------|---------------|----------------|-----------|
| HT_REFCLKP | 66M SE(SE) | 100M DIFF | 100M DIFF | |
| HT_REFCLKN | NC | 100M DIFF | 100M DIFF | |
| REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V) | 100M DIFF |
| REFCLK_N | NC | NC | vref | 100M DIFF |
| GFX_REFCLK* | 100M DIFF | 100M DIFF | 100M DIFF | 100M DIFF |
| GPP_REFCLK | NC | 100M DIFF | 100M DIFF(OUT) | |
| GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF | |

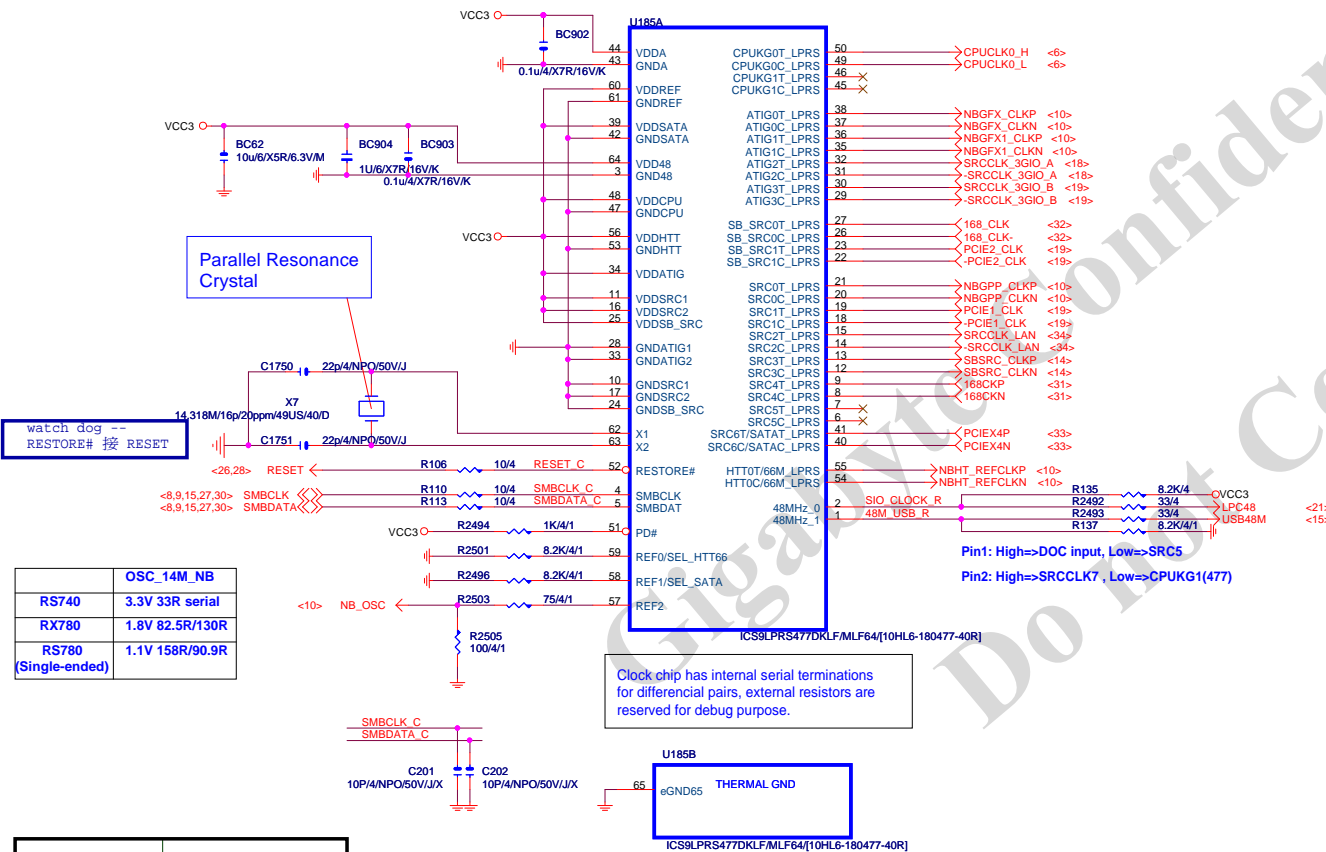
* the GFX_REFCLK input is required for all cases

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



GIGABYTE™

| | | | | | |
|--------|--------------------------|--------------|-------------|----|------|
| Title | | | RTM880N-793 | | |
| Size | Document Number | GA-990XA-UD3 | | | Rev |
| Custom | | | | | 3.03 |
| Date: | Friday, October 19, 2012 | Sheet | 13 | of | 35 |



PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

S.B HEATSINK

SB_HS

SB_HS(12SP2-S0610-11R_12SP2-S0610-12R_12SP2-S0610-13R)

<13> SB5RC_CLKP M23 PCIE_RCLKP/NB_LNK_CLKP
<13> SB5RC_CLKN P23 PCIE_RCLKN/NB_LNK_CLKN

U29 NB_DISP_CLKP
U28 NB_DISP_CLKN

T26 NB_HT_CLKP
T27 NB_HT_CLKN

V21 CPU_HT_CLKP
T21 CPU_HT_CLKN

V23 SLT GFX_CLKP
T23 SLT GFX_CLKN

L29 GPP_CLKOP
L28 GPP_CLKON

N29 GPP_CLK1P
N28 GPP_CLK1N

M29 GPP_CLK2P
M28 GPP_CLK2N

T25 GPP_CLK3P
V25 GPP_CLK3N

L24 GPP_CLK4P
L23 GPP_CLK4N

M25 GPP_CLK5P
M24 GPP_CLK5N

P29 GPP_CLK6P
P28 GPP_CLK6N

N26 GPP_CLK7P
N27 GPP_CLK7N

T29 GPP_CLK8P
T28 GPP_CLK8N

L25 14M_25M_48M_OSC

25MHZ_X1 L26 25M_X1

25MHZ_X2 L27 25M_X2

PR7 1M/4 25MHZ_X2 L27 25M_X2

PC15 22P/4/NPO/50V/J

PC16 22P/4/NPO/50V/J

PC13 18P/4/NPO/50V/J

PC14 18P/4/NPO/50V/J

PC15 22P/4/NPO/50V/J

PC16 22P/4/NPO/50V/J

PC17 22P/4/NPO/50V/J

PC18 22P/4/NPO/50V/J

PC19 22P/4/NPO/50V/J

PC20 22P/4/NPO/50V/J

PC21 22P/4/NPO/50V/J

PC22 22P/4/NPO/50V/J

PC23 22P/4/NPO/50V/J

PC24 22P/4/NPO/50V/J

PC25 22P/4/NPO/50V/J

PC26 22P/4/NPO/50V/J

PC27 22P/4/NPO/50V/J

PC28 22P/4/NPO/50V/J

PC29 22P/4/NPO/50V/J

PC30 22P/4/NPO/50V/J

PC31 22P/4/NPO/50V/J

PC32 22P/4/NPO/50V/J

PC33 22P/4/NPO/50V/J

PC34 22P/4/NPO/50V/J

PC35 22P/4/NPO/50V/J

PC36 22P/4/NPO/50V/J

PC37 22P/4/NPO/50V/J

PC38 22P/4/NPO/50V/J

PC39 22P/4/NPO/50V/J

PC40 22P/4/NPO/50V/J

Part 1 of 5

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

Part 1 of 5

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

Part 1 of 5

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

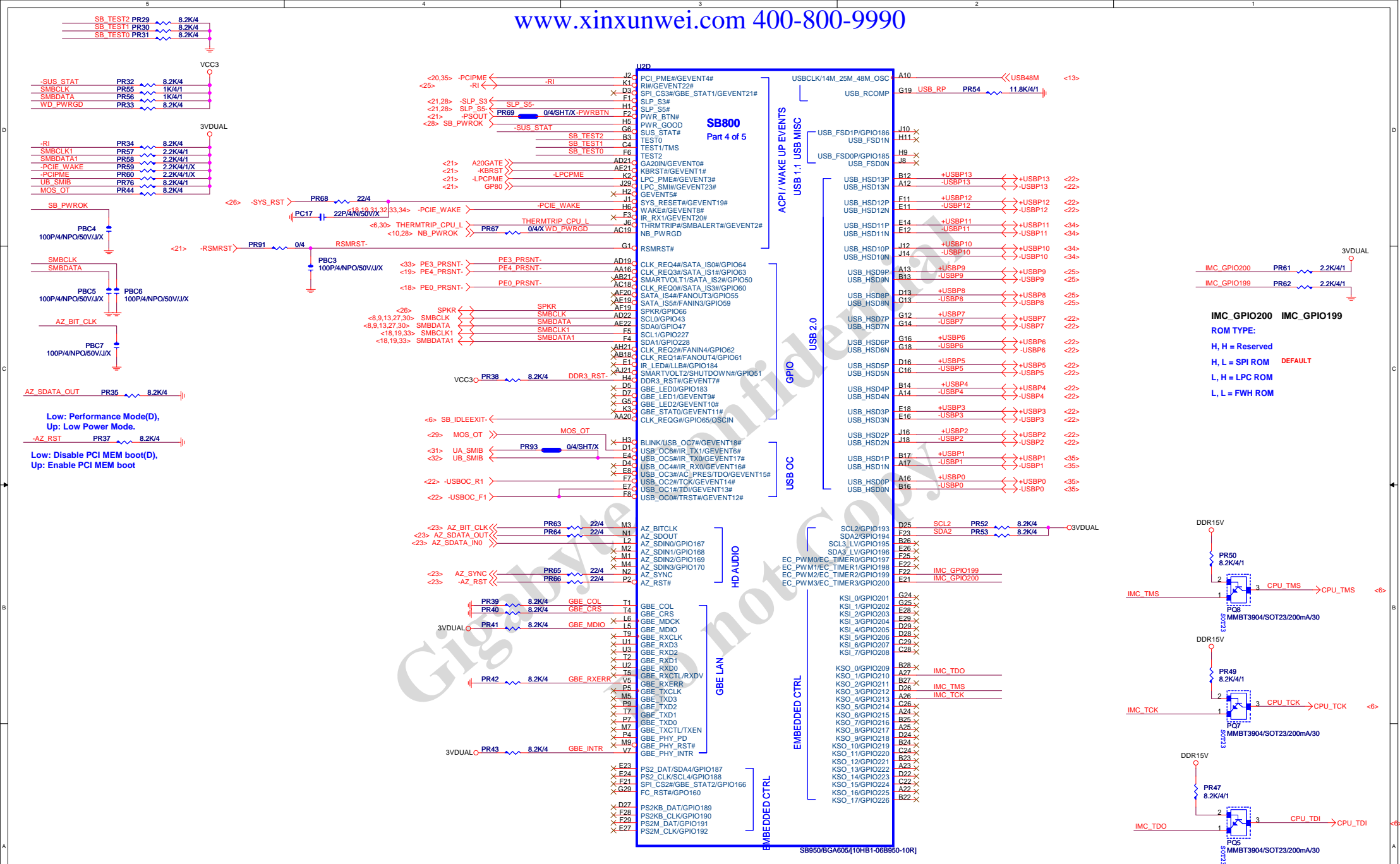
PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#

PCIE_RST#





PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

VCC_SB C PR75 1K/4/1 SATA_CALRP AB14
PR74 931/4/1 SATA_CALRN AA14

<26> -SATA_LED -SATA_LED AD11 SATA_ACT#/GPIO67

AD16 SATA_X1

AC16 SATA_X2

SB SPI DI PR70 22/4 SB SPI DI R J5
SB SPI DO PR71 22/4 SB SPI DO R E2
SB SPI CLK PR72 22/4 SB SPI CLK R K4
SB SPI CS_ITE PR73 22/4 SB SPI CS_ K9
G2

<21> -SB_SPI_CS_ITE

SERIAL ATA
GPIO
HW MONITOR
SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

SPIROM

SB800
Part 2 of 5

SERIAL ATA

GPIO

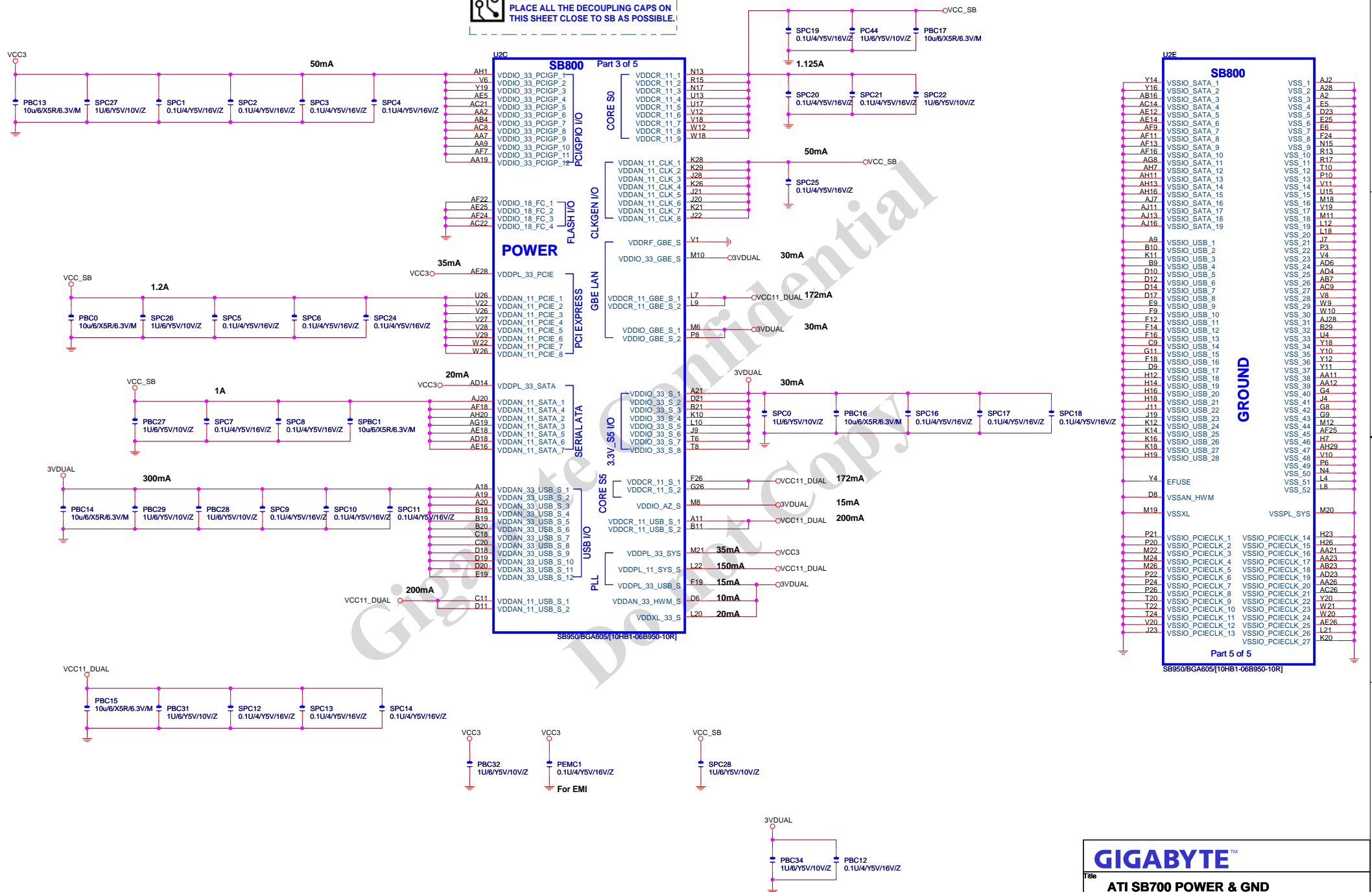
SPIROM

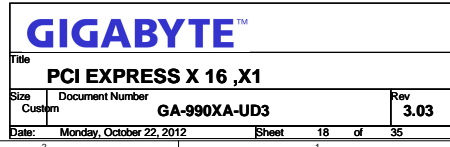
SB800
Part 2 of 5

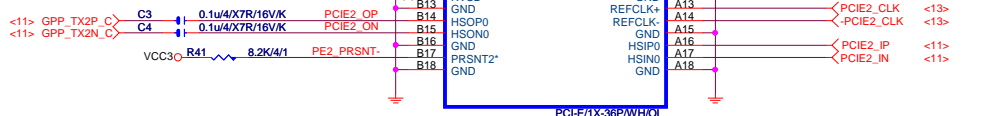
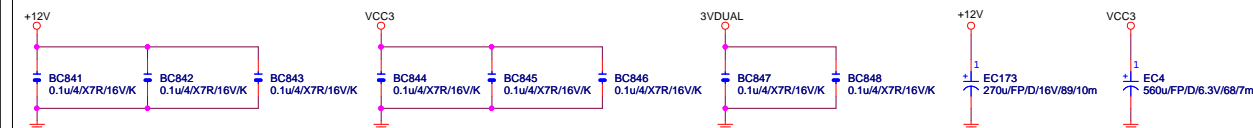
SERIAL ATA



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



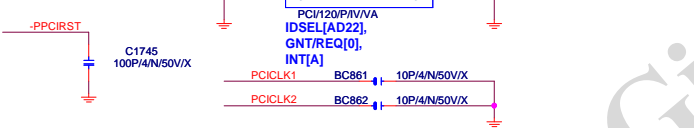
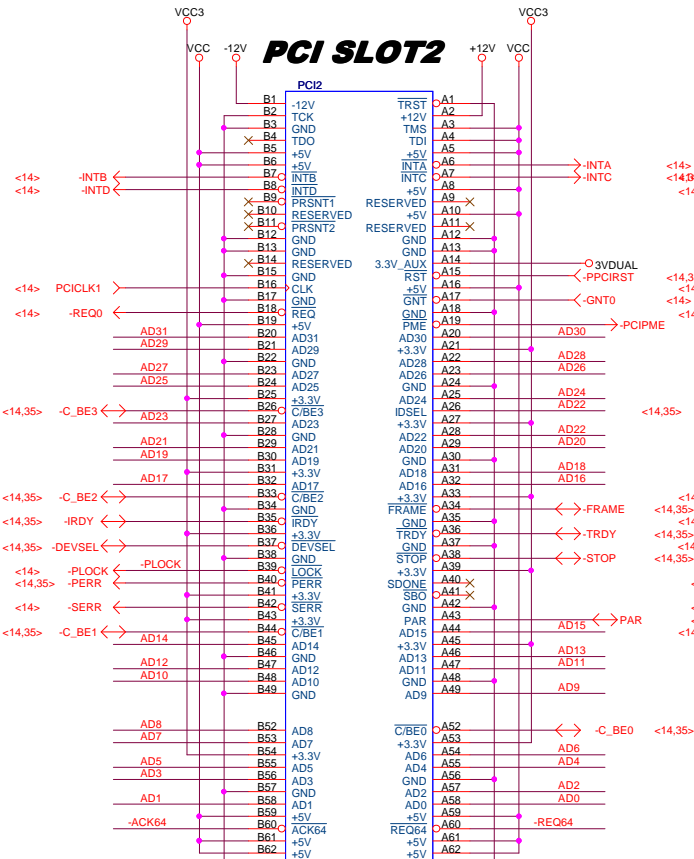




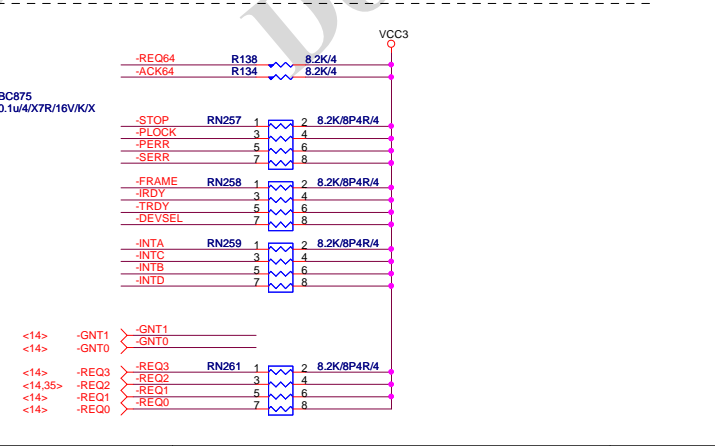
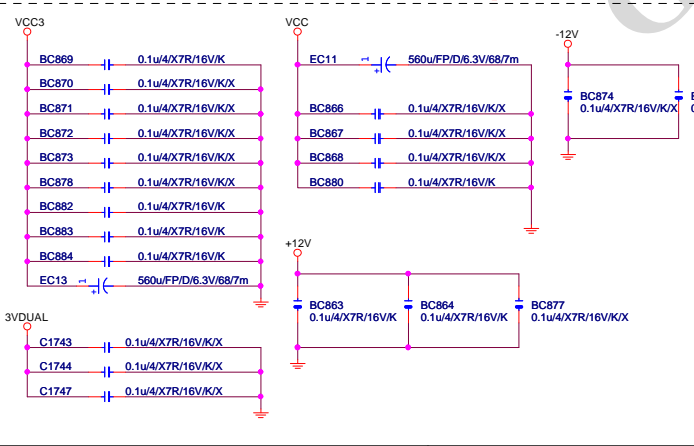
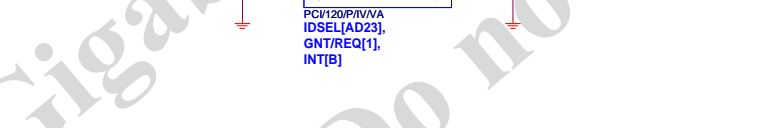
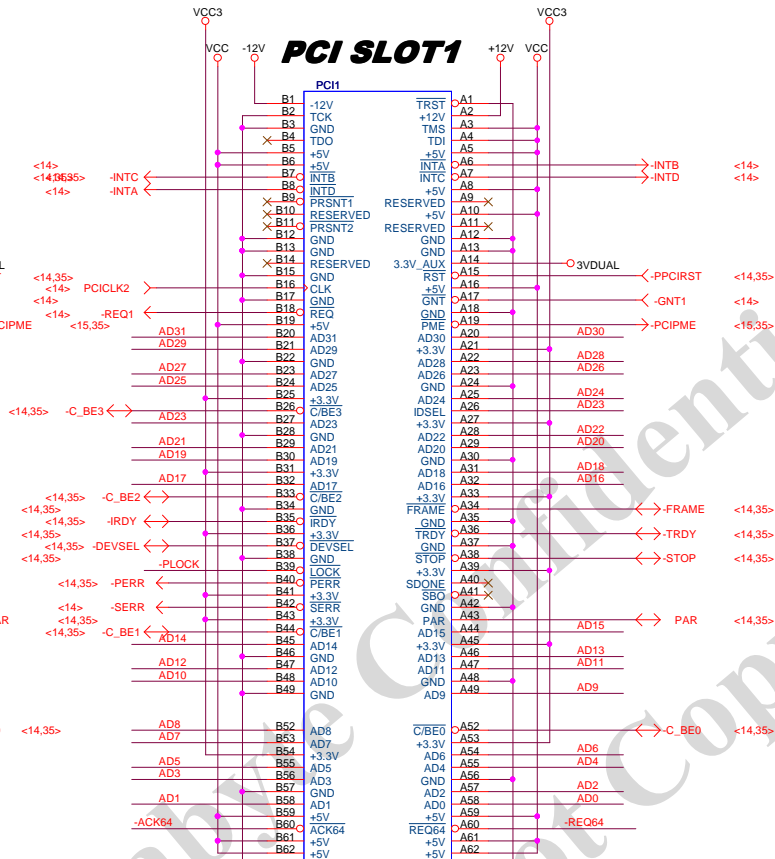
PCI SLOT 1,2

<14,35> AD[0..31] ↔ AD[0..31]

PCI SLOT2



PCI SLOT1

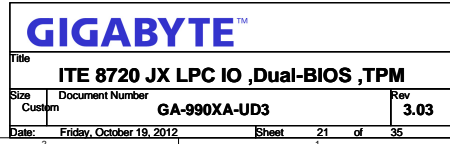


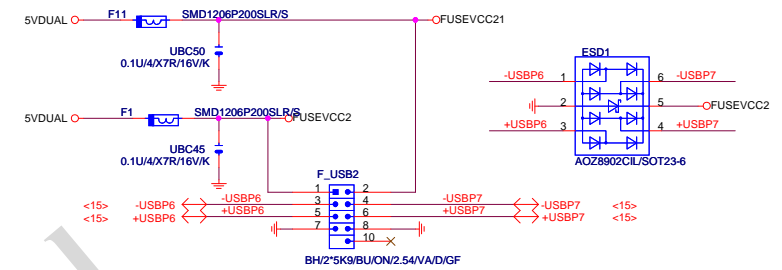
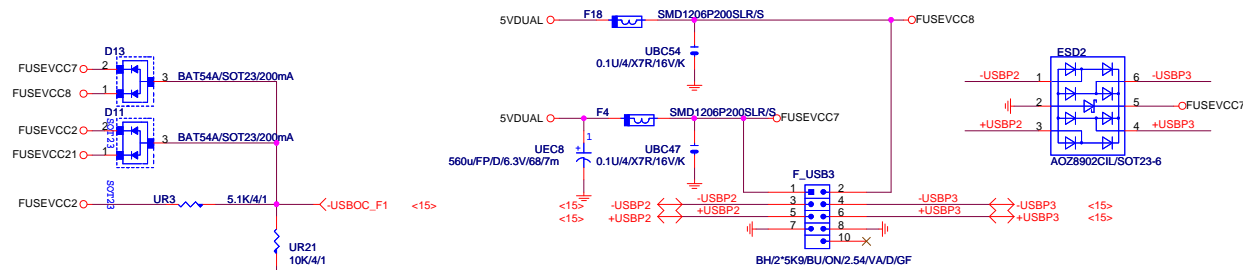
GIGABYTE™

PCI SLOT 1,2,3

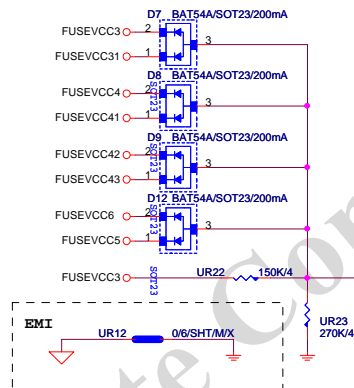
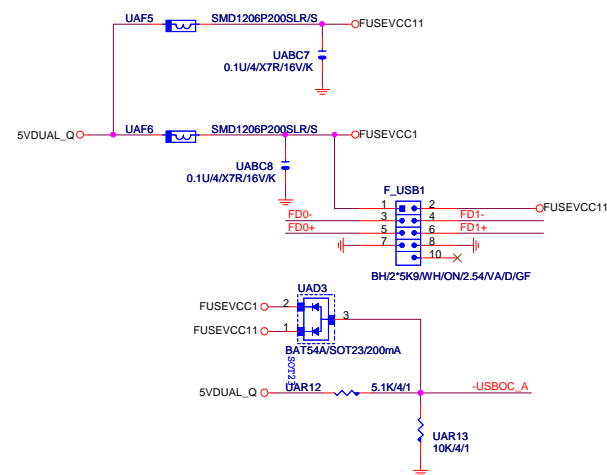
Size Custom Document Number GA-990XA-UD3 Rev 3.03

Date: Friday, October 19, 2012 Sheet 20 of 35

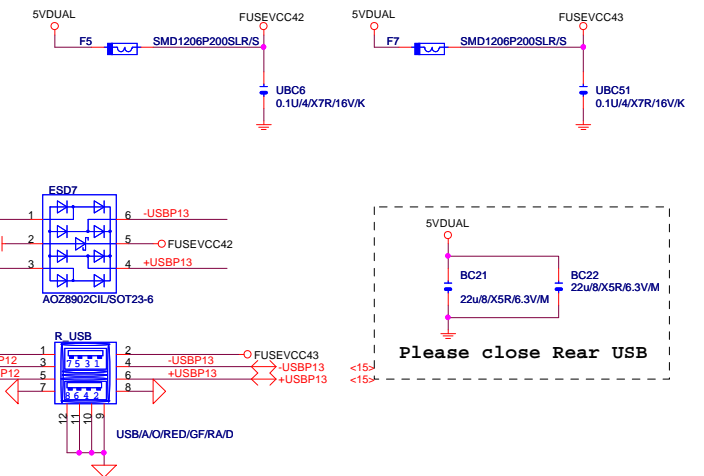




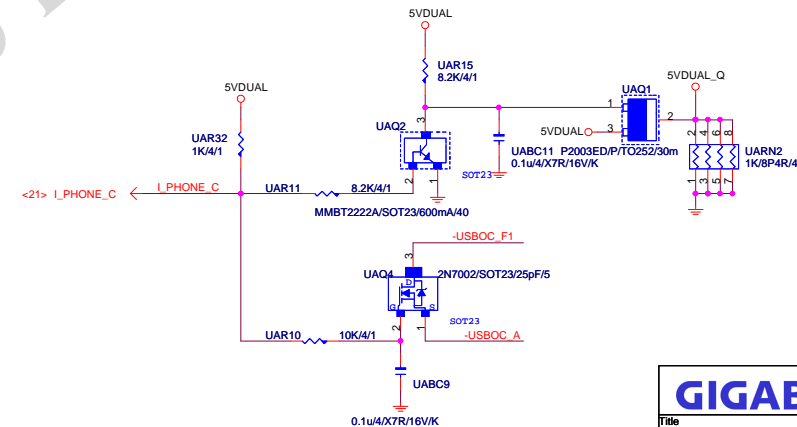
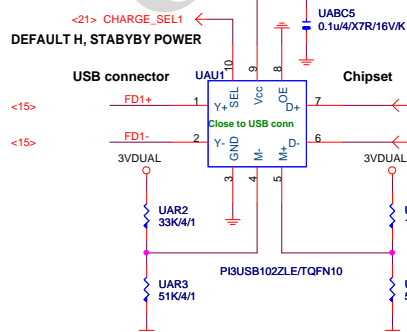
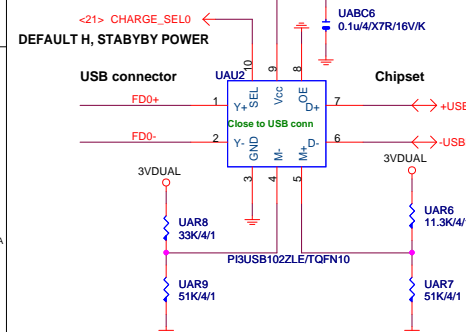
FRONT SIDE USB1



REAR USB



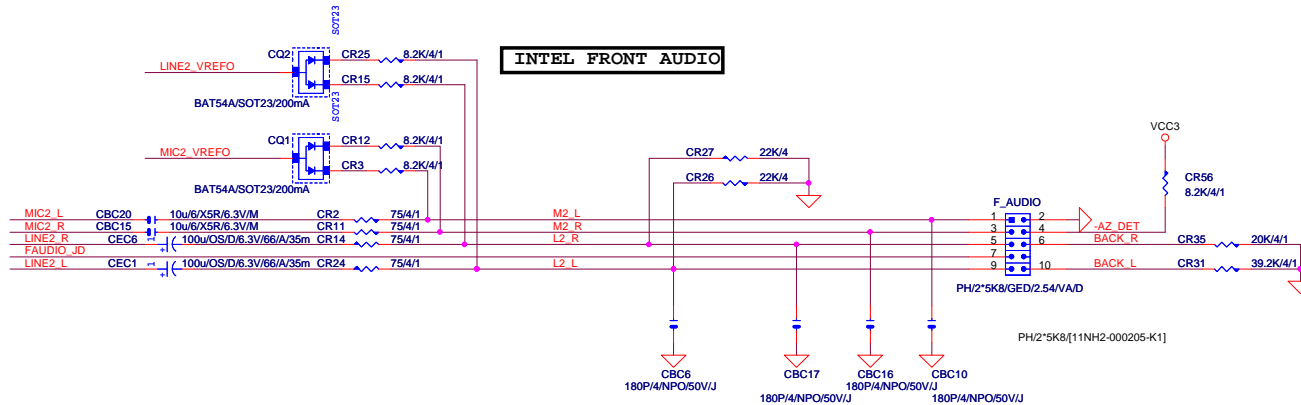
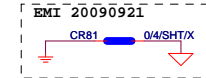
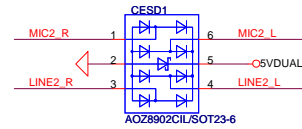
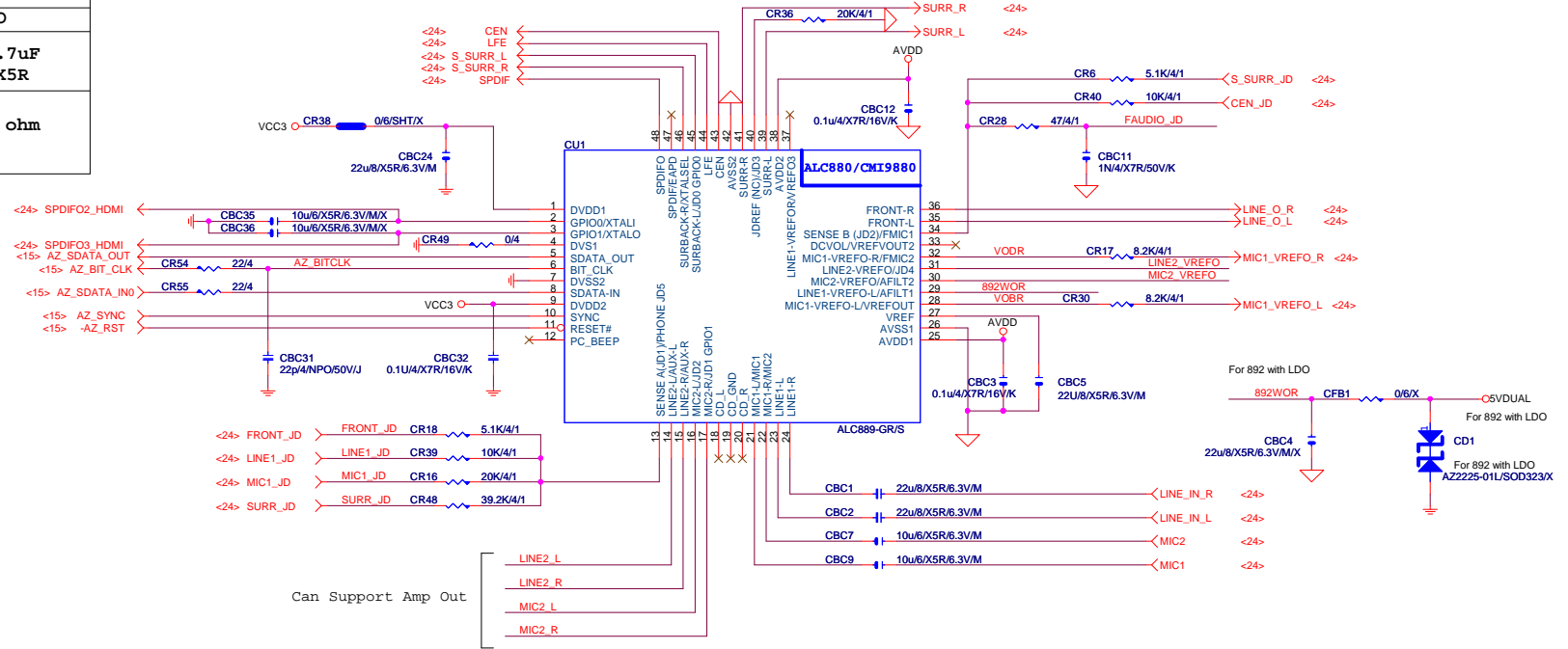
I_Phone charger circuit

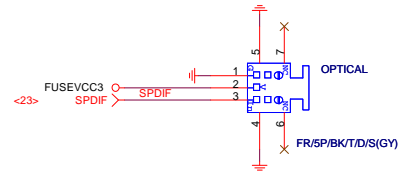
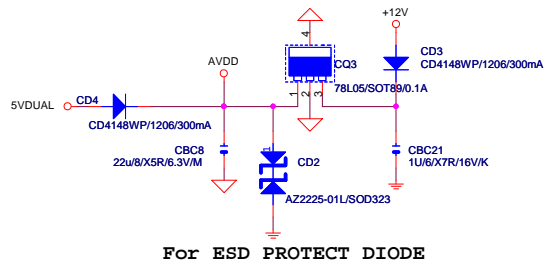
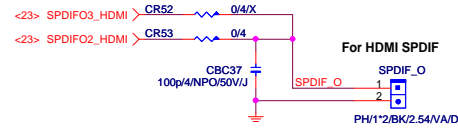
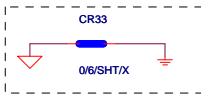


GIGABYTE™

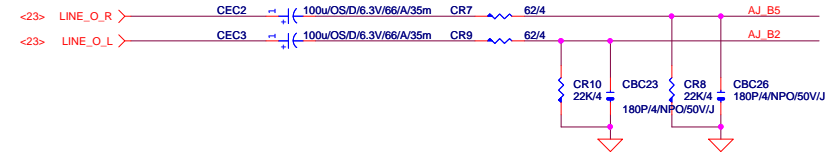
| Title | | |
|--------------------|--------------------------|----------------|
| COM/LPT/F_USB1_PWR | | |
| Size | Document Number | Rev |
| Custom | GA-990XA-UD3 | 3.03 |
| Date: | Friday, October 19, 2012 | Sheet 22 of 35 |

| | ALC892R | ALC889 | ALC889A |
|-------------------------------------------------------------------------------------------|---------------|-----------------------|---------------|
| CR16 | X | X | O |
| CR24 | X | X | O |
| CR25 | X | O | O |
| CBC42 | 10uF/X5R | X | X |
| CR2 | 20K/1% | 20K/1% | 20K/0.1% |
| CR9 | O | O | X |
| CR10 | X | X | O |
| CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45 | 4.7uF /X5R | 10uF /X5R | 4.7uF /X5R |
| CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60 | 75 ohm | 66 ohm or lower | 75 ohm |

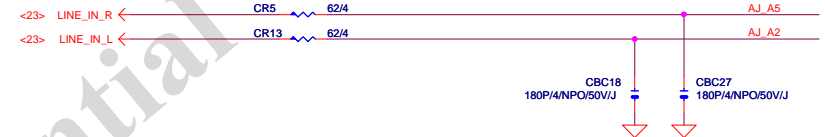




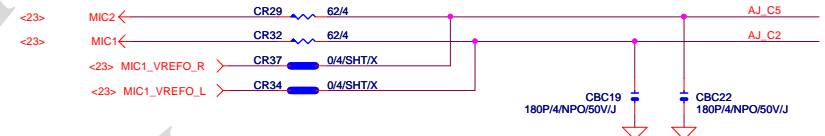
LINE OUT FRONT OUT



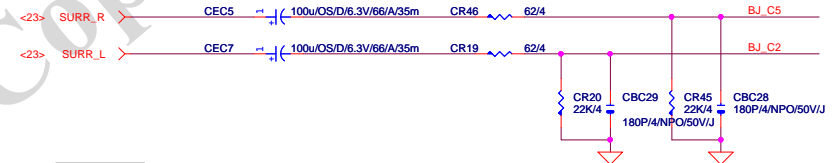
LINE-IN



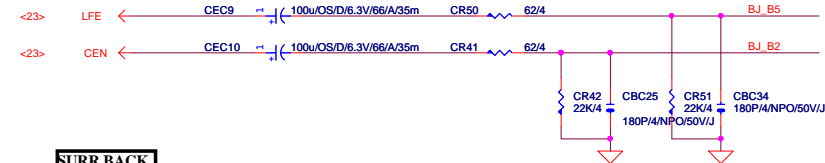
MIC



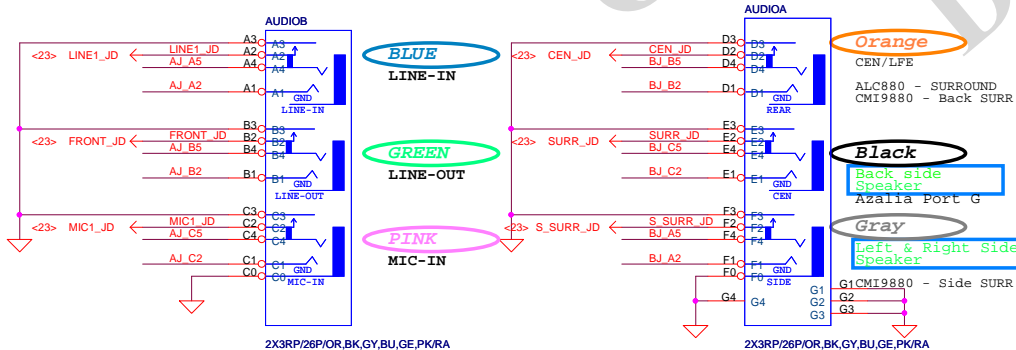
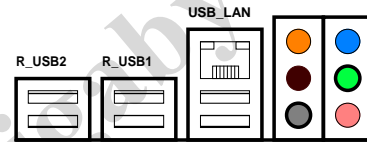
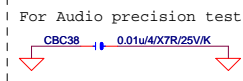
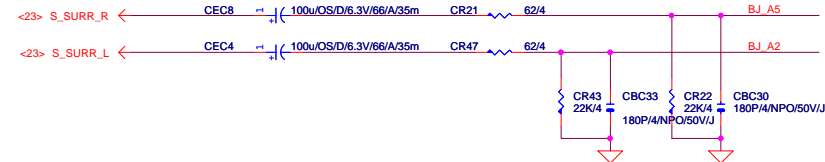
SURROUND



CEN/LFE



SURR BACK



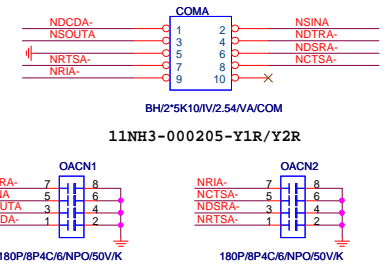
A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7*15P/[11NR6-403004-11]

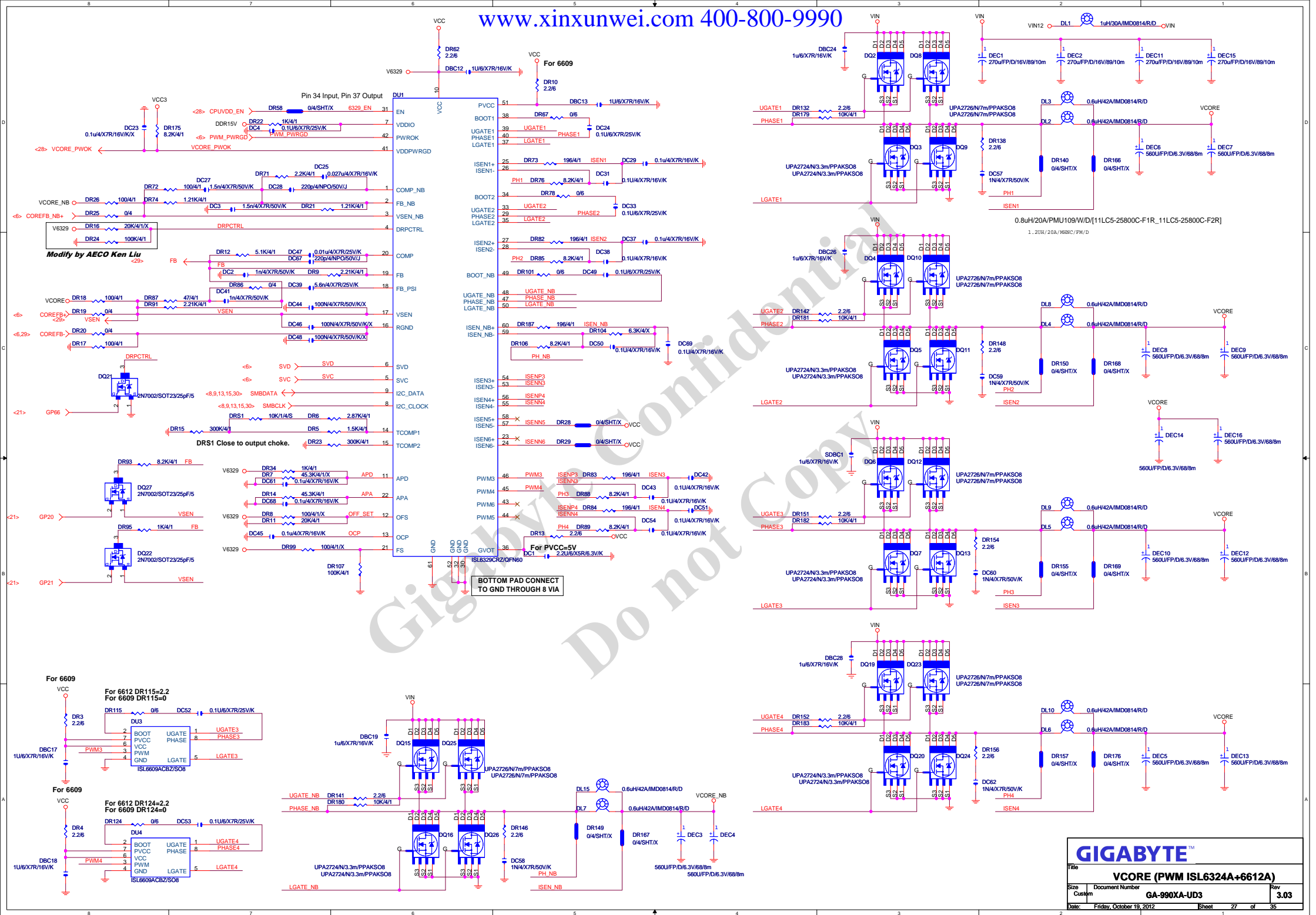
A3R7/13P/0BG/[11NR6-403006-71]
3R7*15P/[11NR6-403004-31]

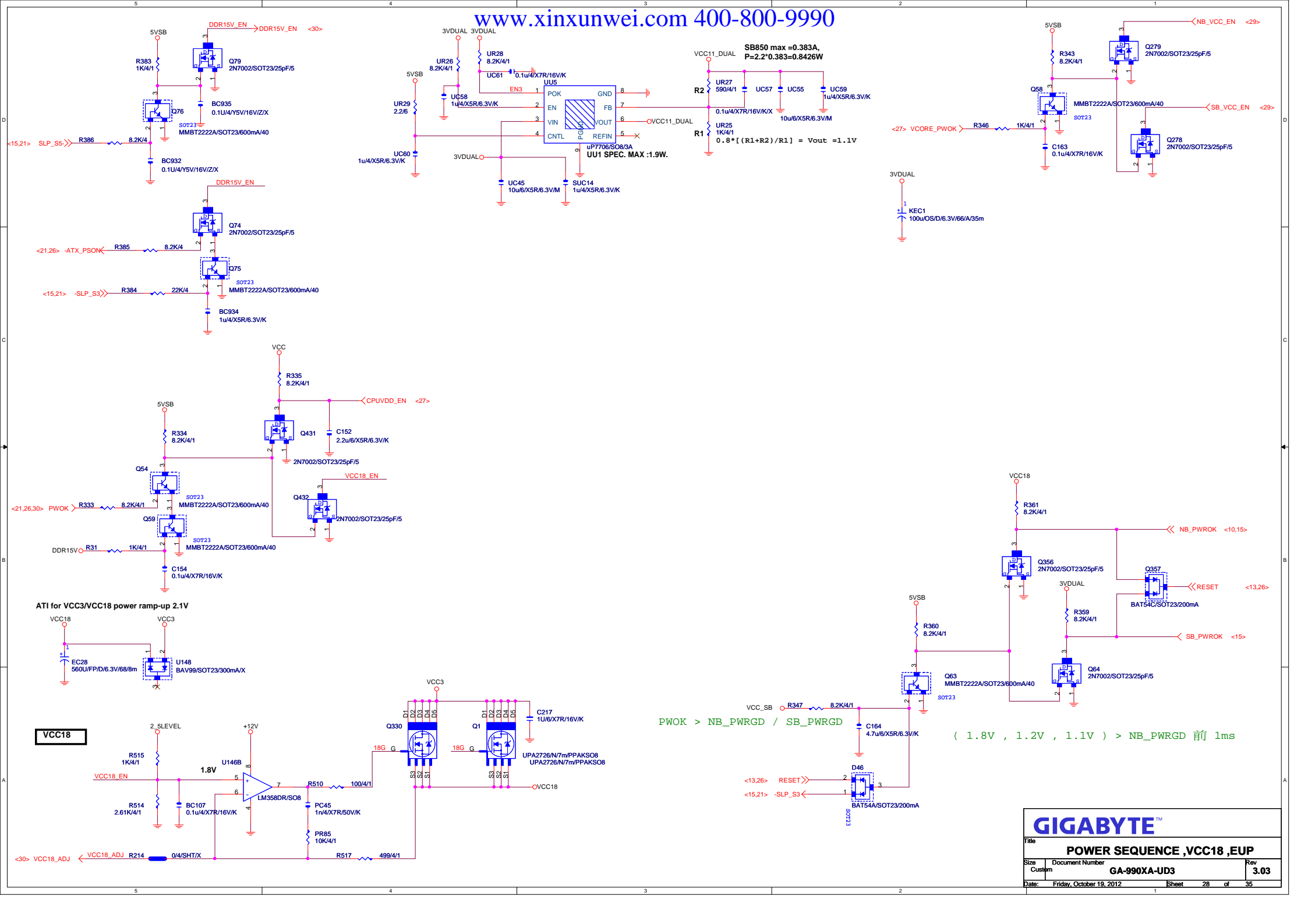
GIGABYTE™

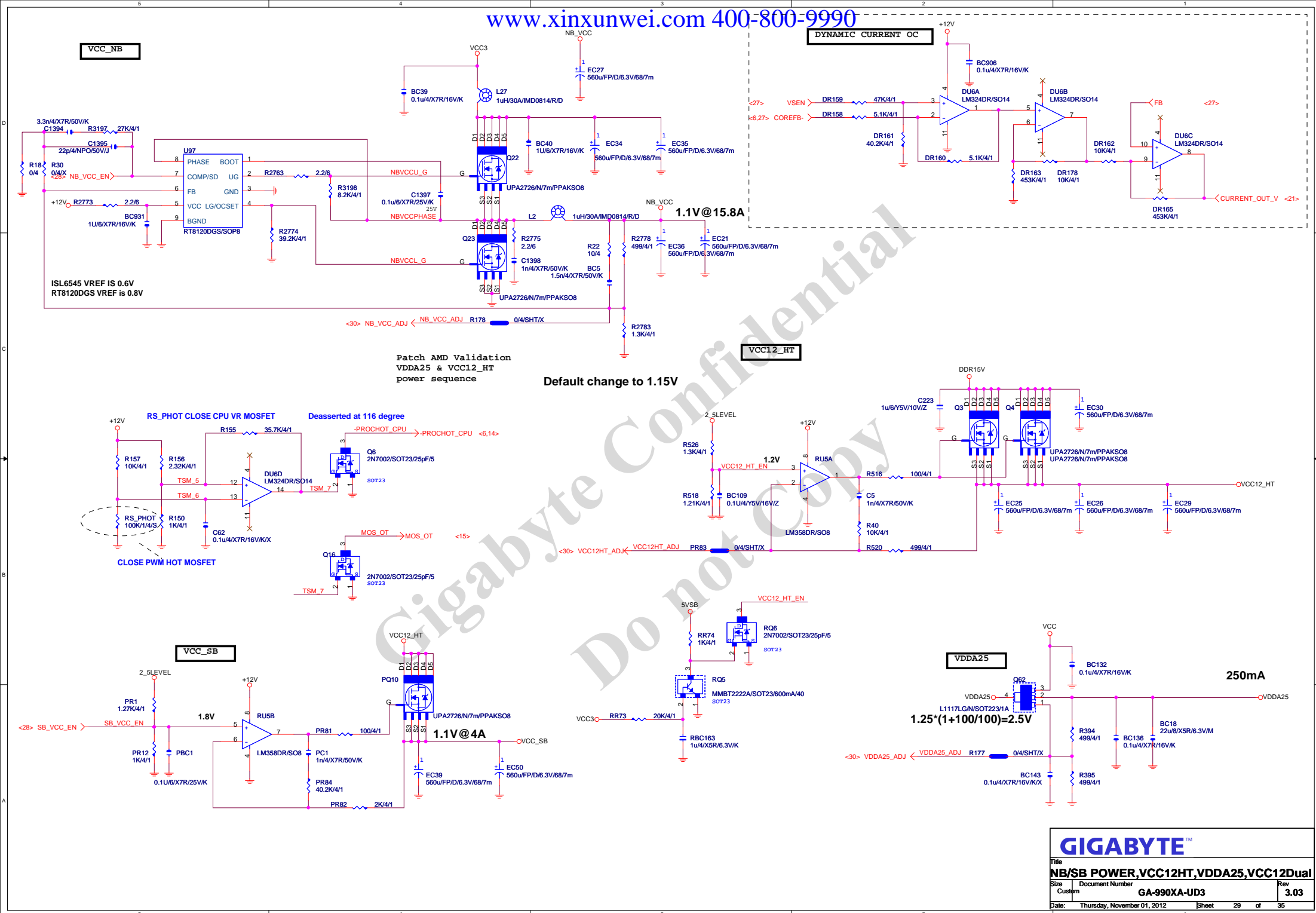
AUDIO JACK

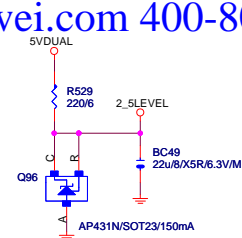
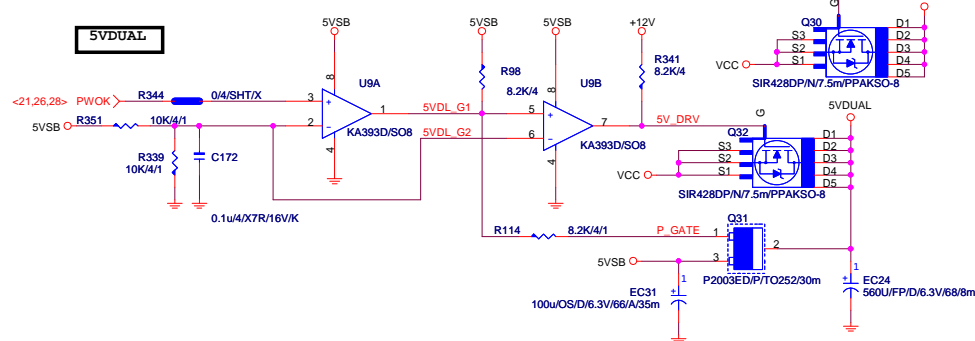
| | | |
|--------|--------------------------|----------------|
| Size | Document Number | Rev |
| Custom | GA-990XA-UD3 | 3.03 |
| Date: | Friday, October 19, 2012 | Sheet 24 of 35 |



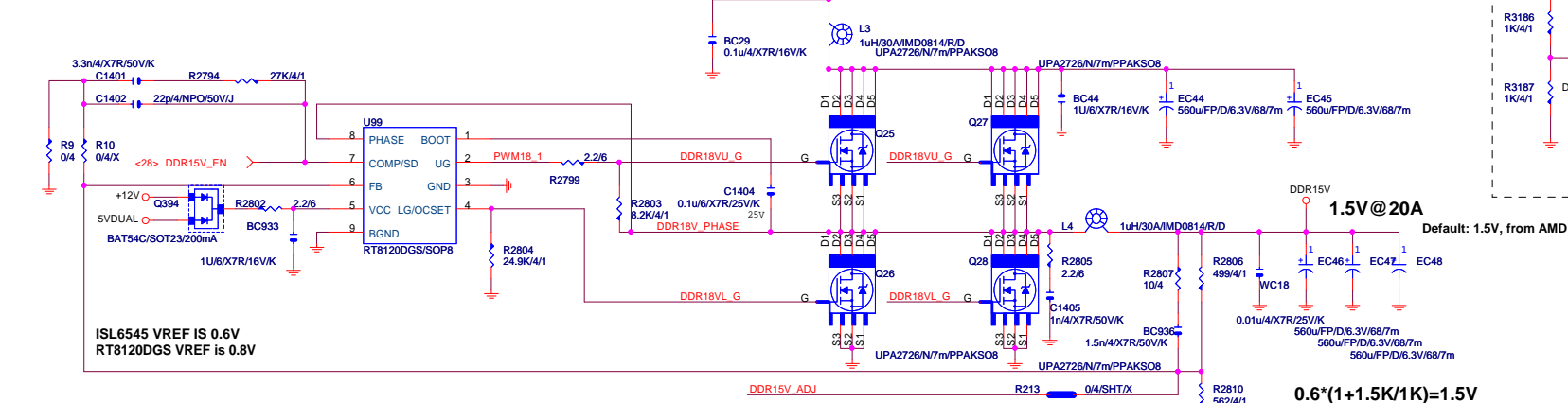
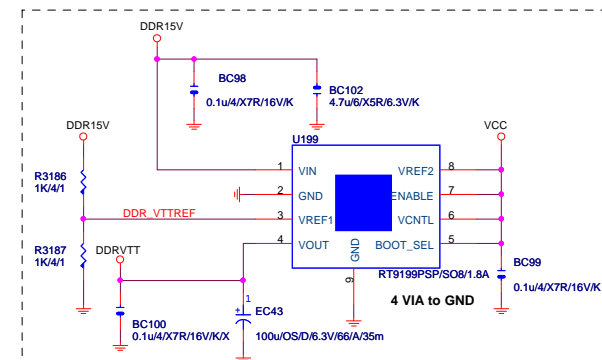
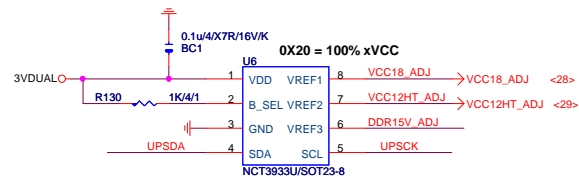
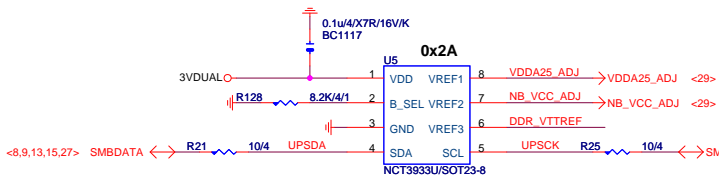
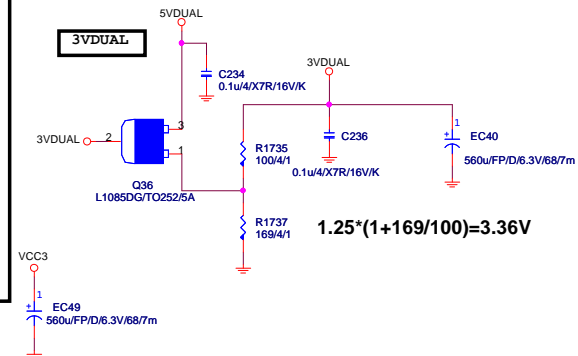
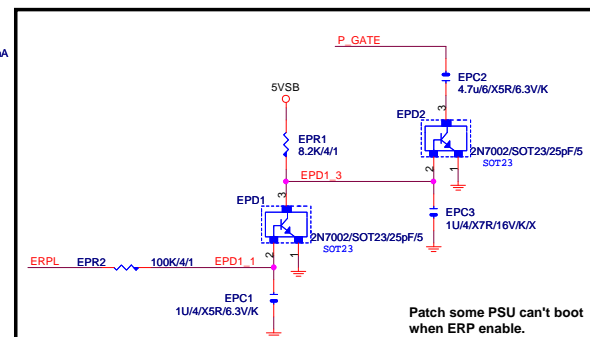
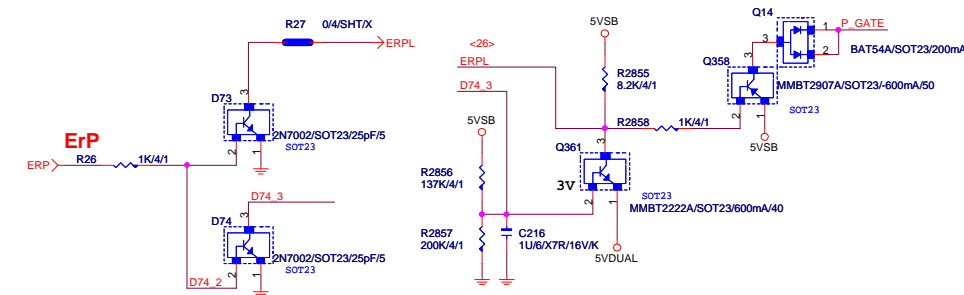
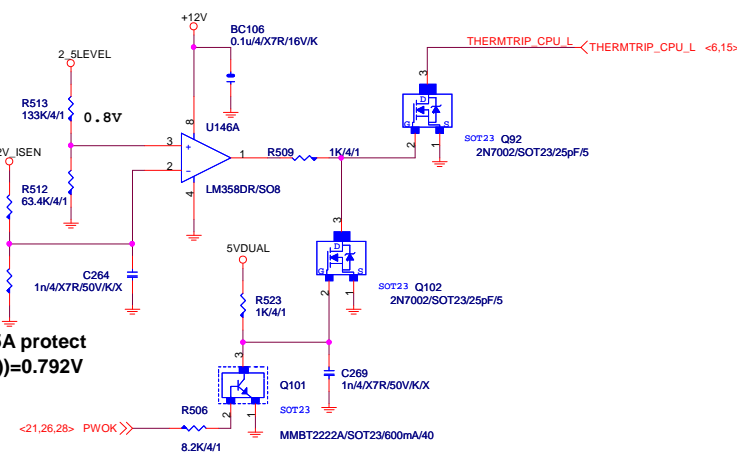


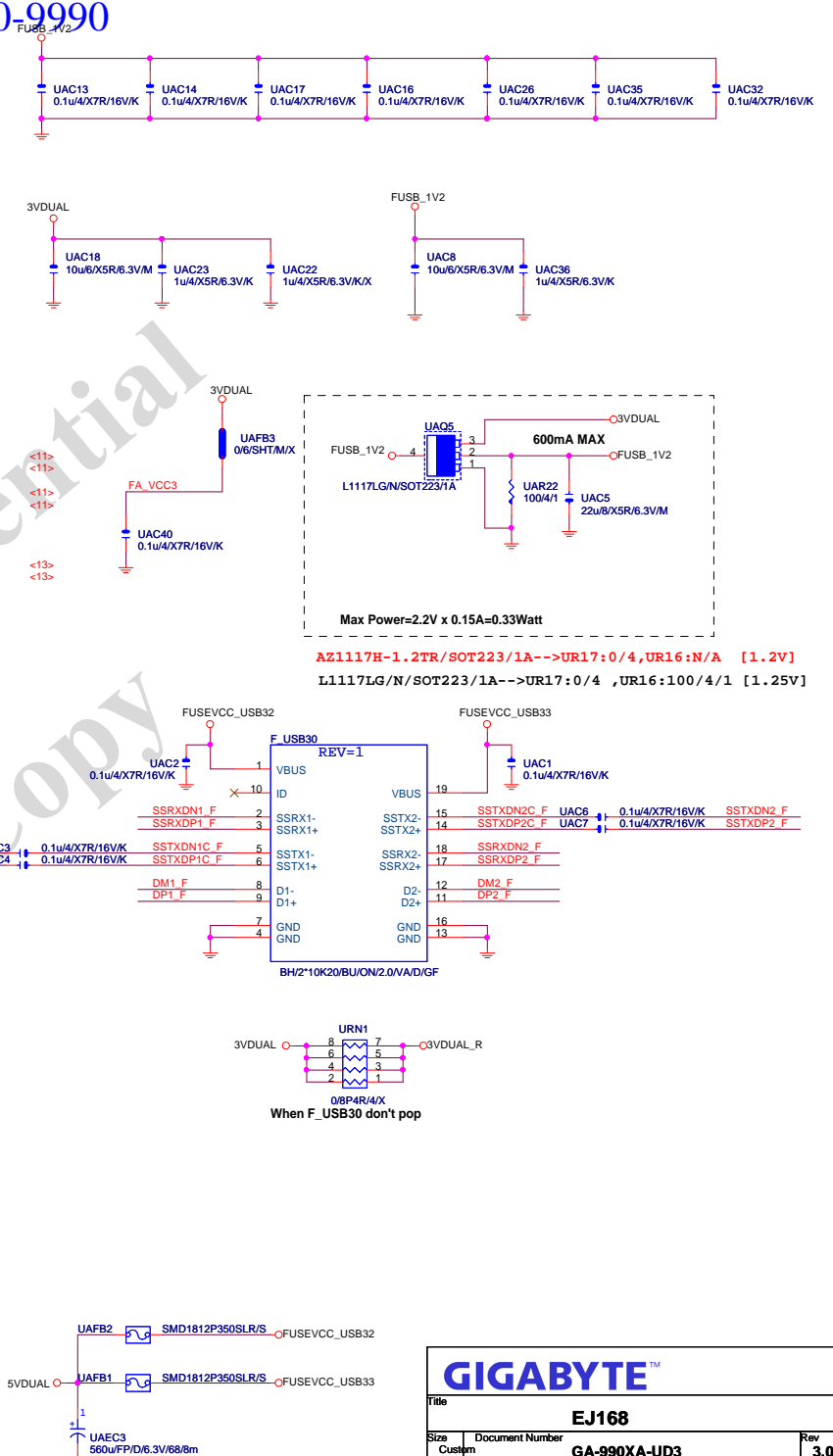
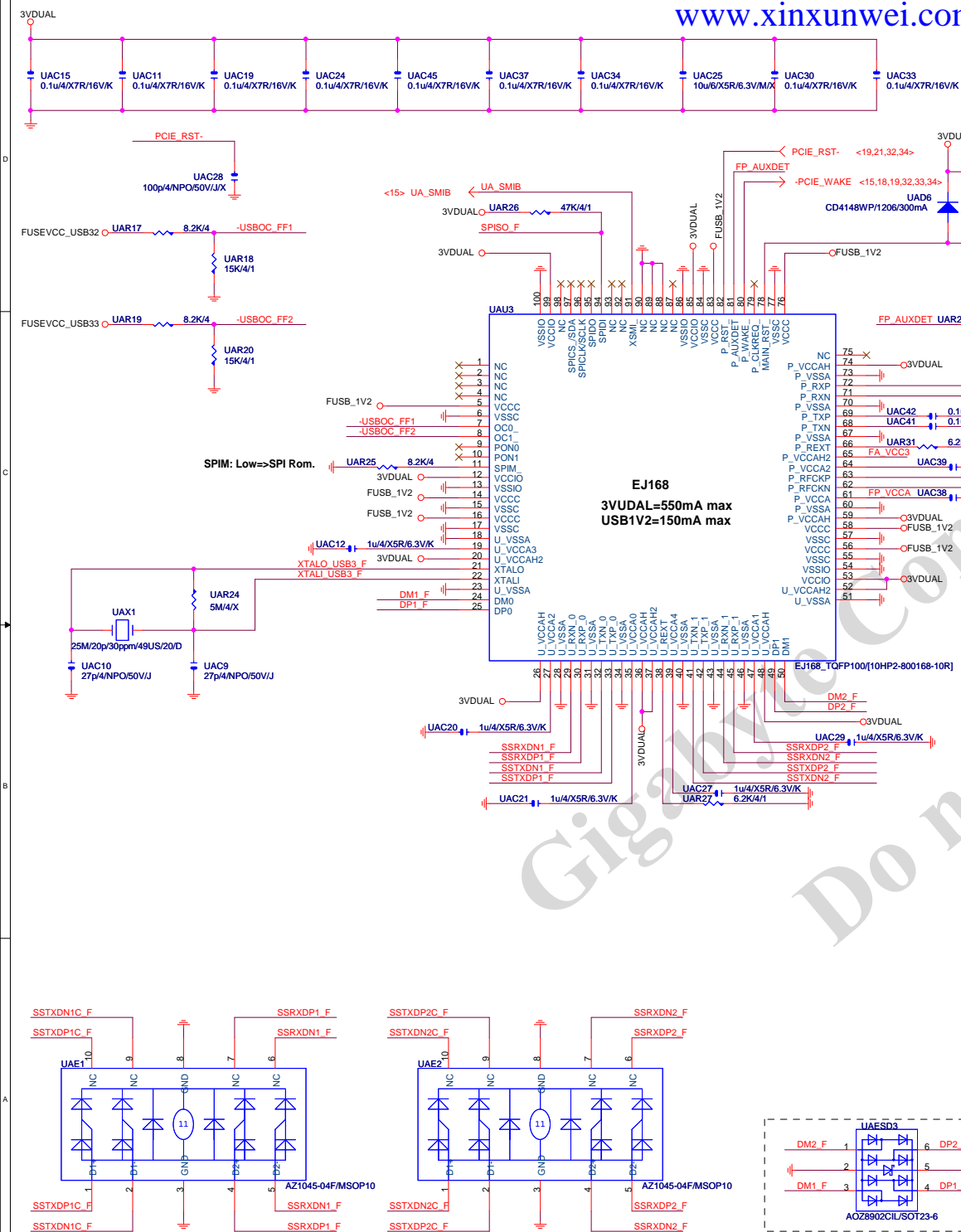






9.5V / 25A protect
 $9.5 \times (1.21K / (13.3K + 1.21K)) = 0.792V$



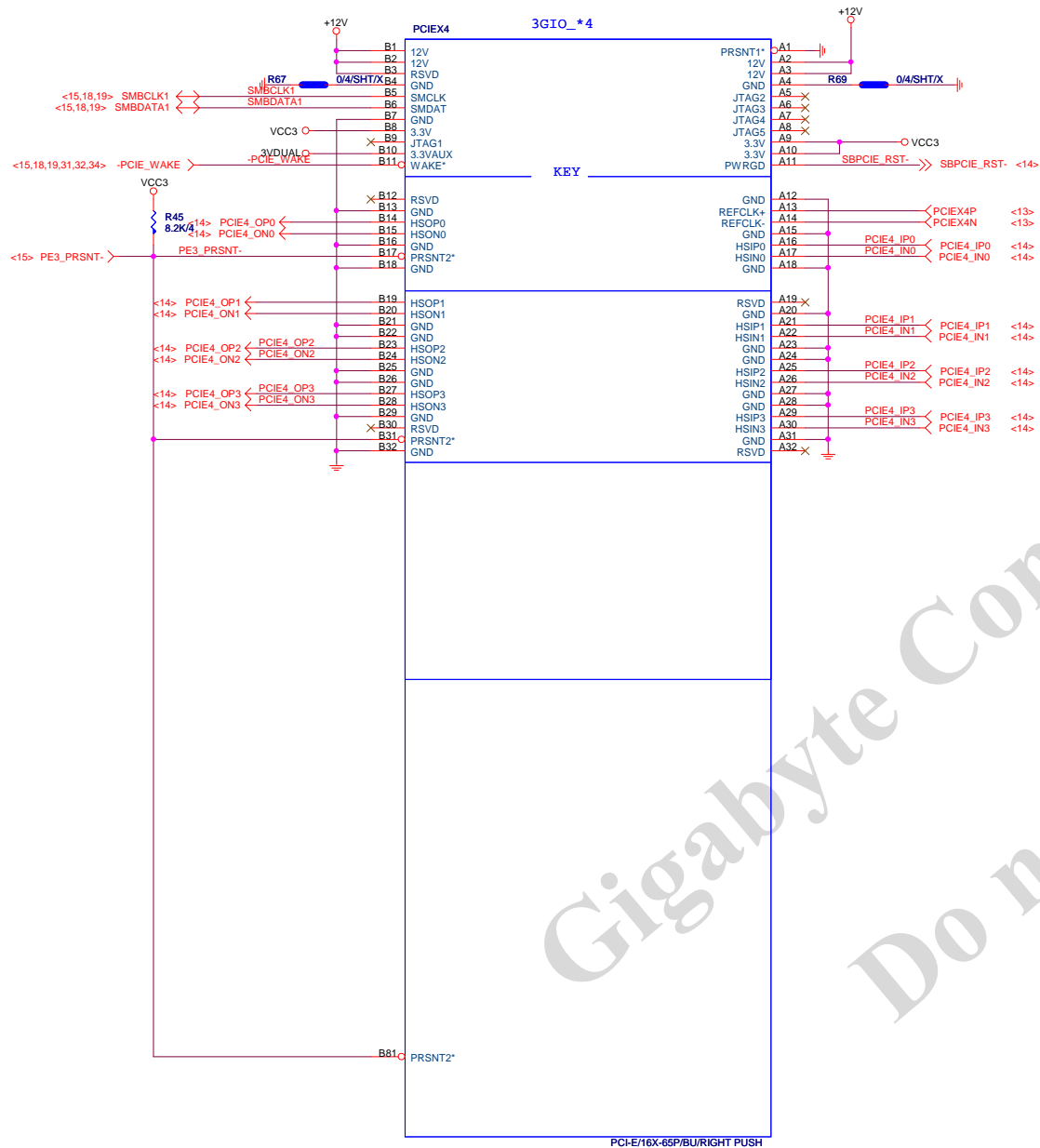


$$\text{BANDWIDTH} = 5\text{GHz} * (8\text{b}/10\text{b}) = 4\text{Gb/s} = 500\text{MB/s}$$

Close to USB30_LAN

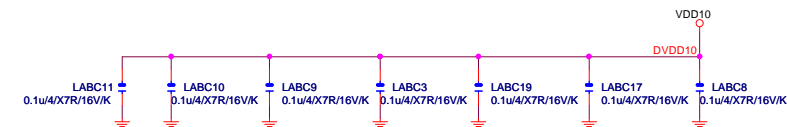
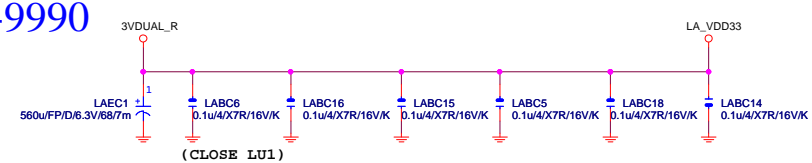
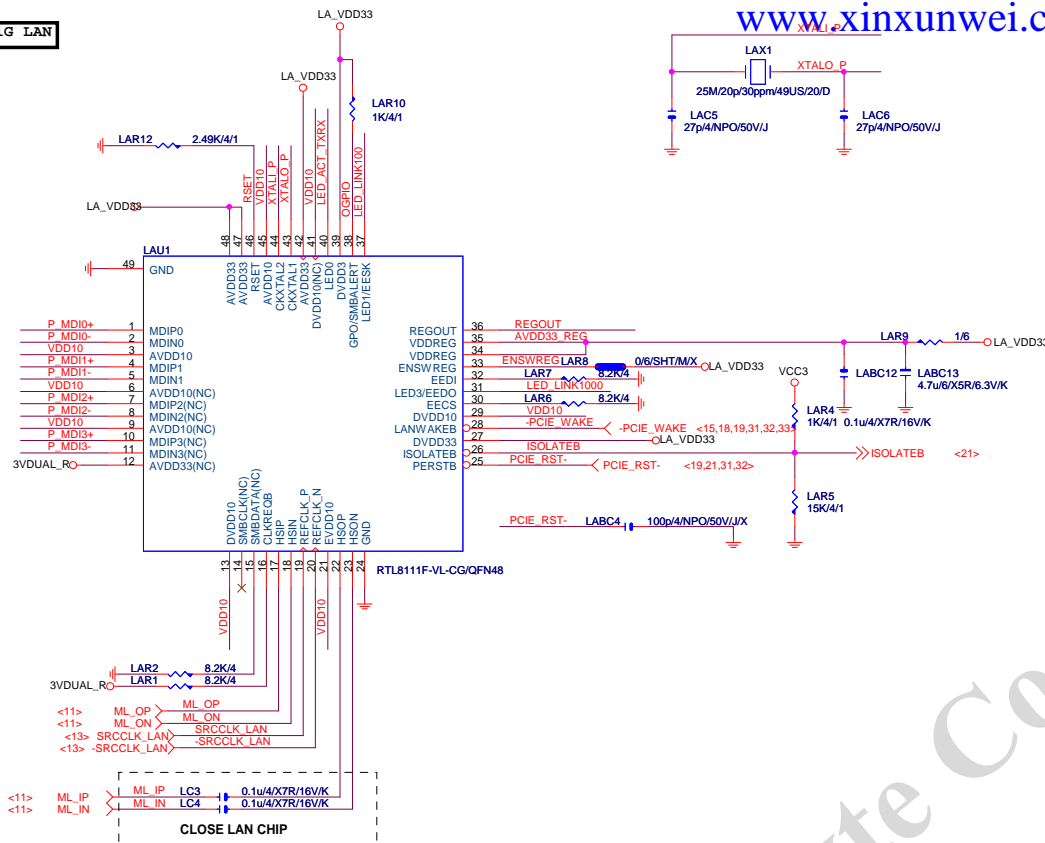
90歐姆:[20/6/5.5/6/20]

| | | | |
|-------------|--------------------------|-------|----------|
| Title | | | |
| EJ168 F_USB | | | |
| Size | Document Number | Rev | |
| Custom | GA-990XA-UD3 | 3.03 | |
| Date: | Friday, October 19, 2012 | Sheet | 32 of 35 |

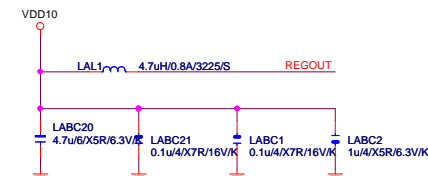
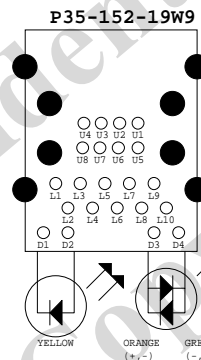


PCIE/16X-65P/BU/RIGHT PUSH

PCIE-1G LAN

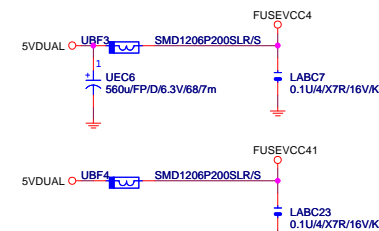
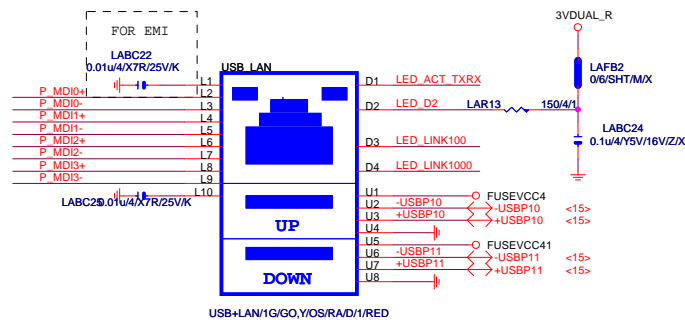


USB_LAN CONNECTOR



USB_LAN

```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O
```



```

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS)  DISABLE MDI-X FUNCTION
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
EMI                                     LR1

```

